MAPMT BOX CONDENSED TIMING DIAGRAM

TCD_5XRS

TCD_D — | TCMD | DCMD | TOKEN2 | TOKEN1 | TOKEN0 | (COMMAND IN ON CABLE FROM TCD)

CMD_REG1 — | TCMD/DCMD/TOKEN | (PARALLEL FORMAT, SYNC'D TO TCD_RS)

CMD_REG2 — | TCMD/DCMD/TOKEN | (PARALLEL FORMAT, SYNC'D TO SYSCLK)

TCD_RS — 25.0 ns (BOX PHASE ADJUST)

CLK/4 — 102.7 ns

CLK

SYNC

ADCCLK

RSTEN — 5.0 ns

RSTDLY — 30.0 ns RST WIDTH — 30.9 ns RST DELAY

RST — 67.7 ns INTEGRATION INTERVAL

RESET PULSES CAN BE SKIPPED, TO PROVIDE
EXTENDED INTEGRATION WINDOW CAPABILITY
FOR DIAGNOSTICS AND/OR SOURCE-MODE CALIBRATION.
MULTIPLE PULSES MAY BE SKIPPED (NOT SHOWN).
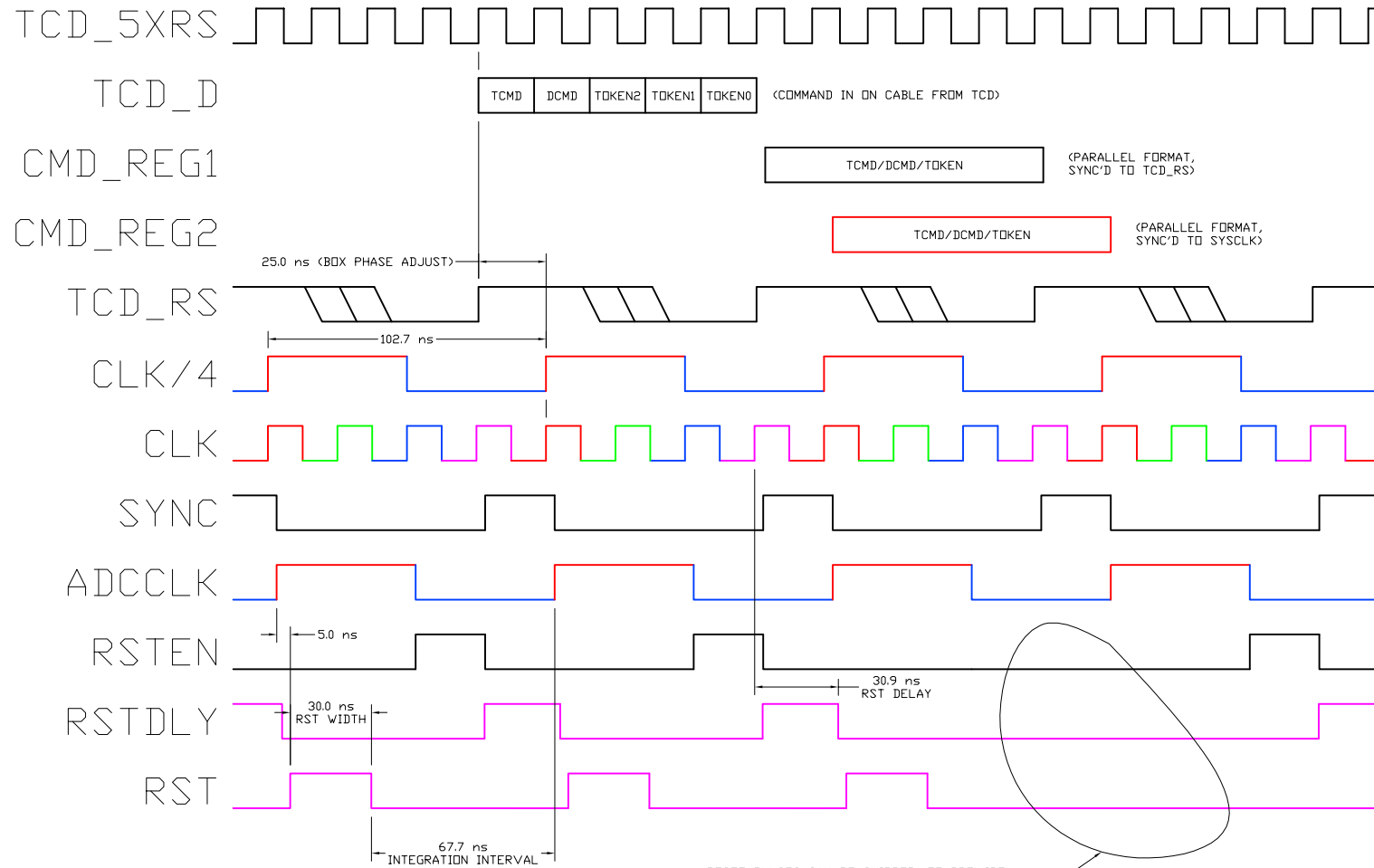
NOTE: BOX PHASE ADJUST, RESET DELAY, AND RESET WIDTH
ARE CONTROLLED BY ADJUSTABLE DELAY CIRCUITS ON RDO BOARD.
VALUES SHOWN ARE 'TYPICAL'. OTHER TIMING VALUES SHOWN ARE
DERIVED/IMPLIED FROM THESE THREE SETTINGS, INPUT CLOCK
PERIOD, AND ESTIMATED FIXED DELAYS IN CIRCUIT.