Implementation of STAR EM-Calorimeter Trigger

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The description of the last e-m calorimeter DSM (EM201) which combines Endcap and Barrel is at the end. PLEASE REFER TO SKIPS WEBPAGE FOR THE GEOMETRY. (Anti-)clockwise and/or lower/higher hour is determined looking from West towards the IP.

1 Layer 0 DSM BEMC-B001,.. and EEMC-E001,...

This DSM layer is the same for Endcap and Barrel East and(!) West. It takes 10 12bit-input channels. It sums up the 6 bit ADC trigger patch values. It places three thresholds on the high tower 6bit ADC values.

Input: 10-12 bit EM-Cal channels
bit (5-0) high tower, bit (11-6) trigger patch

LUT: Pedestal subtraction and energy calibration is done in the EMC readout electronics. Therefore the LUT's are 1:1. Missing/Dead/Non-instrumented channels are zeroed out.

Registers: Three thresholds for 6bit high tower ADC values. THESE THRESHOLDS ARE SIZE ORDERED!, i.e. th2>th1>th0. If the size order is not obeyed, the trigger will not fire.

For the Barrel **BCW and(!) BCE; index:0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18, 0x19, 0x1a, 0x1b, 0x1c, 0x1d, 0x1e**
R0: BEMC-High-Tower-th0 (6)
R1: BEMC-High-Tower-th1 (6)
R2: BEMC-High-Tower-th2 (6)
For the Endcap **EEC; index:0x17, 0x18, 0x19, 0x1a, 0x1b, 0x1c, 0x1d, 0x1e, 0x1f**
R0: EEMC-High-Tower-th0 (6)
R1: EEMC-High-Tower-th1 (6)
R2: EEMC-High-Tower-th2 (6)

Action:

1st latch input

2nd Place three thresholds on each high tower value.
Intermediate trigger patch ADC sum

3rd 'or' threshold bits for all 10 high-towers
Code the three thresholds into two bits
('00' ADC<th0, '01' ADC>th0, '10' ADC > th1, '11' ADC>th3)
total ADC sum for trigger patches

4th Latch output

Output: (9-0) ADC-sum Trigger patches
(11-10) high-tower threshold bits
(15-12) empty

2 Layer 0 DSM BEMC-B(E/W)003-8-13

This DSM layer is similar to BEMC-B001. The input is split into to two separate 0.2x1.0 jet patches.

Input: 10x12 bit channels. The two 0.2 patches are labeled J1 and J3.
Even input channels J1: ch0/2/4/6/8; odd channels J3: ch1/3/5/7/9
The geometry/position for J1 and J3 is swaped between East and West, which plays a role when forming jet-patches in layer1.

West	J1	clockwise side, higher hour	J3	anti-clockwise side, lower hour
East	J3	clockwise side, higher hour	J1	anti-clockwise side, lower hour

LUT: 1:1; Zero out missing channels

Registers: Three thresholds for 6bit high tower adc values. These thresholds are identical to BEMC-B001 and the indices's are listed there.

Action: same as BB001

Output: Two cables:
J3: West=Anti-clockwise/low hour; East=clockwise/high hour
(8-0) ADC-sum Trigger patches J3
(9) empty (sum one bit shorter than in BB001)
(11-10) high-tower threshold bits J3
(15-12) empty
J1: West=Clockwise/high hour; East=anti-clockwise/low hour
(24-16) ADC-sum Trigger patches J1
(25) empty (sum shorter than BB001)
(27-26) high-tower threshold bits J1
(31-28) empty

3 Layer 0 DSM EEMC-E002-5-8

This DSM layer is similar to BB/EE001. The input is split into to two separate 0.3x1.0 6-tower jet patches.

Input: 10x12 bit channels. The two 0.3x1 patches are labeled (J0 anti-clockwise side/low hour) and J1 (clockwise side/high hour) J0: ch0/1/2/3/4 J1: ch5/6/7/8/9

LUT: Pedestal subtraction and energy calibration

Registers: Three thresholds for 6bit high tower adc values. These thresholds are identical to EEMC-E001, the indices's are listed there.

Action: same as BB/EE001

Output: Two cables:
Anti-clockwise part/low hour
(8-0) ADC-sum Trigger patches J0
(9) empty (sum one bit shorter than in BB001)
(11-10) high-tower threshold bits J0
(15-12) empty
Clockwise part/high hour
(24-16) ADC-sum Trigger patches J1
(25) empty (sum shorter than BB001)
(27-26) high-tower threshold bits J1
(31-28) empty

4 Layer 1 DSM BEMC-B(E/W)101-103

This layer combines two 1x1 barrel jet patches (jp0-anti-clockwise/lower hour and jp1-clockwise/higher hour), combines their high tower bits and and places thresholds on their adc sums. There are two different algorithms for east and west to take care of the switch in geometry position of the j1/j3 half modules from input channels ch2 and ch3.

Input ch0-B001 - 0.4x1.0
ch1-B002 - 0.4x1,0
ch2-B003 - lower bits, j3 0.2x1.0 West:anti-clockwise; East:clockwise
ch3-B003 - upper bits, j1 0.2x1.0 West: clockwise; East: anti-clockwise
ch4-B004 - 0.4x1.0
ch5-B005 - 0.4x1.0
ch6/7 not used
same for B006-15 and East Barrel

from B001/002/004/005
(9-0) = TP adc sum
(10-11 = HT threshold bits
(15-12)= empty
from B003
(8-0) = TP adc sum j3
(9) = empty
(10-11)= HT threshold bits j3
(15-12)= empty
(24-16)= TP adc sum j1
(25) = empty
(27-26)= HT threshold bits j1

(31-28)= empty

LUT: 1:1

Registers: **BC1, index East 0x21, 0x10,0x11; West 0x12, 0x13, 0x14** Three thresholds for 12bit trigger patch adc values
R0: BEMC-Jet-Patch-th0 (12)
R1: BEMC-Jet-Patch-th1 (12)
R2: BEMC-Jet-Patch-th2 (12)

Action: for both jet patches jp0 and jp1 SEPARATELY:
sum the ADC sums from the trigger patches to 1x1 jet patch energies (12 bits)
place three Jet-Patch ADC thresholds on those sums
sum both jet patch energies to a **13 bit** energy sum for the 2x1 barrel segment
code the three thresholds into two bits
combine the high tower bits

Output: (7-0) UPPER EIGHT bits of the total energy sum
(9-8) ADC threshold bits jet patch jp0
(11-10) ADC threshold bits jet patch jp1
(13-12) High tower threshold bits jp0
(15-14) High tower threshold bits jp1

5 Layer 1 DSM EEMC-E101/E102

This layer combines three 0.9x1 Endcap patches, combines their high tower bits and places thresholds on their adc sums.

Input: (E101)
ch0-E001 - 0.6x1.0
ch1-E002 - 0.3x1,0 bits(15-0), jp0 anti-clockwise
ch2-E002 - 0.3x1.0 bits(31-16),jp1 clockwise
ch3-E003 - 0.6x1.0
ch4-E004 - 0.6x1.0
ch5-E005 - 0.3x1.0 bits(15-0), jp0 anti clockwise
ch6/7 not used

Input: (E102)
ch0-E005 - 0.3x1.0 bits(31-16),jp1 clockwise
ch1-E006 - 0.6x1,0
ch2-E007 - 0.6x1.0
ch3-E008 - 0.3x1.0 bits(15-0), jp0 anti-clockwise
ch4-E008 - 0.3x1.0 bits(31-16),jp1 clockwise
ch5-E009 - 0.6x1.0
ch6/7 not used

from E001/003/004/006/007/009
(9-0) = TP adc sum
(10-11 = HT threshold bits
(15-12)= empty
from B002/005/008
(8-0) = TP adc sum j0
(9) = empty
(10-11)= HT threshold bits j0
(15-12)= empty
(24-16)= TP adc sum j1
(25) = empty
(27-26)= HT threshold bits j1
(31-28)= empty

LUT: 1:1

Registers: **EEC; index lower half 0x15, upper 0x16 (not in 2003)** Three thresholds for 11bit 1x0.9 jet patch adc sum
R0: EEMC-Jet-Patch-th0 (11)
R1: EEMC-Jet-Patch-th1 (11)
R2: EEMC-Jet-Patch-th2 (11)

Action: for all three jet patches jp0,jp1 and jp3 SEPARATELY:
sum the ADC sums from the trigger patches to 0.9x1 jet patch energies (11 bits)
place three Jet-Patch ADC thresholds on those sums
sum both jet patch energies to a **13 bit** energy sum for the 3x0.9 end cap segment
code the three thresholds into two bits
combine the high tower bits

Output: (7-0) UPPER EIGHT bits of the total energy sum
(9-8) ADC threshold bits jet patch jp0 - 4'clock /10' (E102)
(11-10) ADC threshold bits jet patch jp1 -6'clock/12' (E102)
(13-12) ADC threshold bits jet patch jp2 -8'clock /02'(E102)
(15-14) High tower threshold bits jp0/1/2 combined

6 Layer 2 DSM L1-EM201 (2004)

This is the third layer for the EMC tree for **polarized proton (spin) triggers, and default for 2004**. The threshold bits for end cap and barrel are going -separately- into the TCU. **I had trouble placing and routing this module, therefore the total energy sum triggers for endcap and barrel and the jetpatch-topology trigger are presently disabled. J/psi trigger is working.**

Input ch0- 1.0x2.0 BEMC-BE101 10' and 12'
ch1- 1.0x2.0 BEMC-BE102 2' and 4'

ch2- 1.0x2.0 BEMC-BE103 6' and 8'
ch3- 1.0x2.0 BEMC-BW101 10' and 12'
ch4- 1.0x2.0 BEMC-BW102 2' and 4'
ch5- 1.0x2.0 BEMC-BW103 6' and 8'
ch6- 0.9x3.0 EEMC-E101 4', 6' and 8'
ch7- 0.9x3.0 EEMC-E102 10', 12' and 2'

from B101/102/103
(7-0) = TP adc sum upper 8 bits
(9-8) = TP threshold bits jp0 (lower hour)
(11-10)= TP threshold bits jp1 (higher hour)
(13-12)= HT threshold bits jp0 (lower hour)
(15-14)= HT threshold bits jp1 (higher hour)
from E101/102 (7-0) = TP adc sum upper 8 bits
(9-8) = TP threshold bits jp0 (4'/10')
(11-10)= TP threshold bits jp1 (6'/12')
(13-12)= TP threshold bits jp2 (8'/2')
(15-14)= HT threshold bits 4'-8' combined

LUT: '1:1'

Registers: **L1; index: 0x1a** Eight thresholds and mode setting bits, for explanation see below

(L1; ind:)

R0:	BEMC-Energy-Sum-th0 (11)
R1:	EEMC-Energy-Sum-th0 (9)
R2:	Threshold-Select-jpsi:(2) values: 0-th0,1-th1,2-th2,**3-jpsi off** Select which BEMC-High-Tower threshold (BEMC-B001,B003-8-13:R0-R2) is used for for jpsi-topology trigger.
R3:	Threshold-Select-jetPatchTopology (2) values: 0,1,2 Select which BEMC/EEMC-Jet Patch threshold (BEMC-B101-103,E101:R0-R2) is used for for adjacent jet patch trigger.
R4:	Trigger-Mode-jetPatchTopology (2) Select Mode for Adjacent Jet patch trigger '00':off '01': trg-jp-tpy=adjacent patches in Barrel '10': trg-jp-tpy=adjacent patches in Endcap '11': trg-jp-tpy=adjacent patches in Barrel or End-cab or between Endcap and Barrel.

Action: sum the jet patch energies for the three 2x1 Barrel segments
place threshold eBarrel > BEMC-Energy-Sum-th0 (R0)
place threshold eEndcap > EEMC-Energy-Sum-th0 (R1)
Select the energy trigger with register 2 (see description of R2)

Combine the 1x1 (0.9x1) jet patch energy thresholds bits for Endcap and barrel. Register 3 selects if we trigger on barrel only, Endcap only, or barrel 'or'

eEndcap.

Combine the high tower threshold bits for Endcap and barrel. Register 4 selects if we use barrel only, Endcap only, or barrel 'or' eEndcap.

The jpsi trigger uses only the high tower threshold bits of the **WEST** barrel. Register 5 selects ONE of the high-tower thresholds (th0,th1,th0 i.e. Reg0-2 of BEMC-001...) for the jpsi-topology trigger. The jpsi trigger fires if two opposite jet patches have high towers above the selected threshold:
– vector bits (0-5) correspond to positions 2,4,6,8,10,12 o'clock

jpsi-trigger = (ht-jpsi(0) and (ht-jpsi(2) or ht-jpsi(3) or ht-jpsi(4))) or
(ht-jpsi(1) and (ht-jpsi(3) or ht-jpsi(4) or ht-jpsi(5))) or
(ht-jpsi(2) and (ht-jpsi(4) or ht-jpsi(5))) or
(ht-jpsi(3) and ht-jpsi(5))

The adjacent jet patch trigger can use the jet patch energy sum threshold bits of the **WEST** barrel and the Endcap. Register 6 selects (presently) ONE of the jet patch ADC sum thresholds (BEMC101-1003,E101 Registers R0-R2) for the adjacent jet patch trigger. For adjacent barrel and Endcap jet patches and adjacent patches between barrel and Endcap a trigger condition is build as follows
bits in jp-tpyB(0-5) correspond to barrel patches 2,4,6,8,10,12 o'clock
bits in jp-tpyE(1-3) correspond to Endcap patches 4,6,8 o'clock
adjacent patches in the barrel

jp-topologyB= (jp-tpyB(0) and jp-tpyB(1)) or
(jp-tpyB(1) and jp-tpyB(2)) or
(jp-tpyB(2) and jp-tpyB(3)) or
(jp-tpyB(3) and jp-tpyB(4)) or
(jp-tpyB(4) and jp-tpyB(5)) or
(jp-tpyB(5) and jp-tpyB(0))

adjacent in Endcap

jp-topologyE= (jp-tpyE(1) and jp-tpyE(2)) or
(jp-tpyE(2) and jp-tpyE(3))

adjacent patches between barrel and Endcap

jp-topologyEB= (jp-tpyB(1) and jp-tpyE(1)) or
(jp-tpyB(2) and jp-tpyE(2)) or
(jp-tpyB(3) and jp-tpyE(3))

Register 7 selects if we trigger on the barrel only, Endcap only or on both and their overlap.

Output: **Available in the last DSM/TCU!**
EEmc and bemc are kept seperate and getseperate bits in the TCU

(1-0) jet patch trigger bits BARREL
(3-2) high tower trigger bits BARREL
(4) energy trigger BARREL
(5) jpsi topology (presently Barrel West)
(6) jet patch topology (Barrel or Endcap)
(8-7) jet patch trigger bits ENDCAP
(10-9) high tower trigger bits ENDCAP
(11) energy trigger ENDCAP

(15-12) empty