STAR SCA/ADC Datasheet

DRAFT - Preliminary

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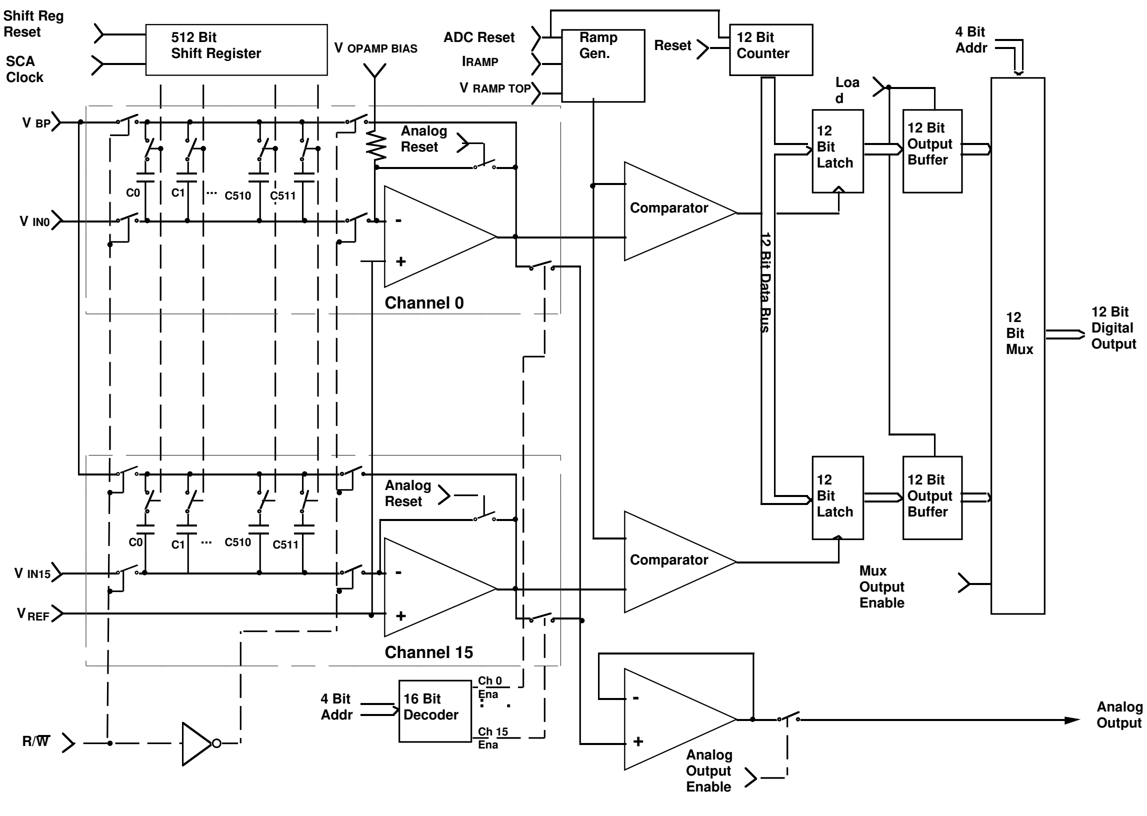
General Description

The NA49-STAR Switched Capacitor Array / Analog to Digital Converter [SCA/ADC,] is a custom IC developed at Lawrence Berkeley Laboratory for use in the NA49 [CERN] and STAR [BNL] Time Projection Chamber front end electronics. The SCA/ADC is a 16 channel device. Each channel consists of 512 switched capacitor sample and holds, followed by a 12 bit analog to digital converter The digital output is buffered and multiplexed.

Required external components are limited to supply and reference decoupling capacitors, and three external resistors to set the ADC ramp current and bias currents ($R_{IRAMP,}$ Op Amp Bias and Comparator Bias). The SCA/ADC requires +5V [digital] and +5V [analog] supply voltages and typically dissipates 100mW.

Three (3) external reference voltages need to be supplied (V_{REF}, $V_{BOTTOM\ PLATE}$, and $V_{RAMP\ TOP}$)

Functional Block Diagram



STAR COMBINED SWITCHED CAPACITOR ARRAY - ADC IC [SCA IC]
BLOCK DIAGRAM

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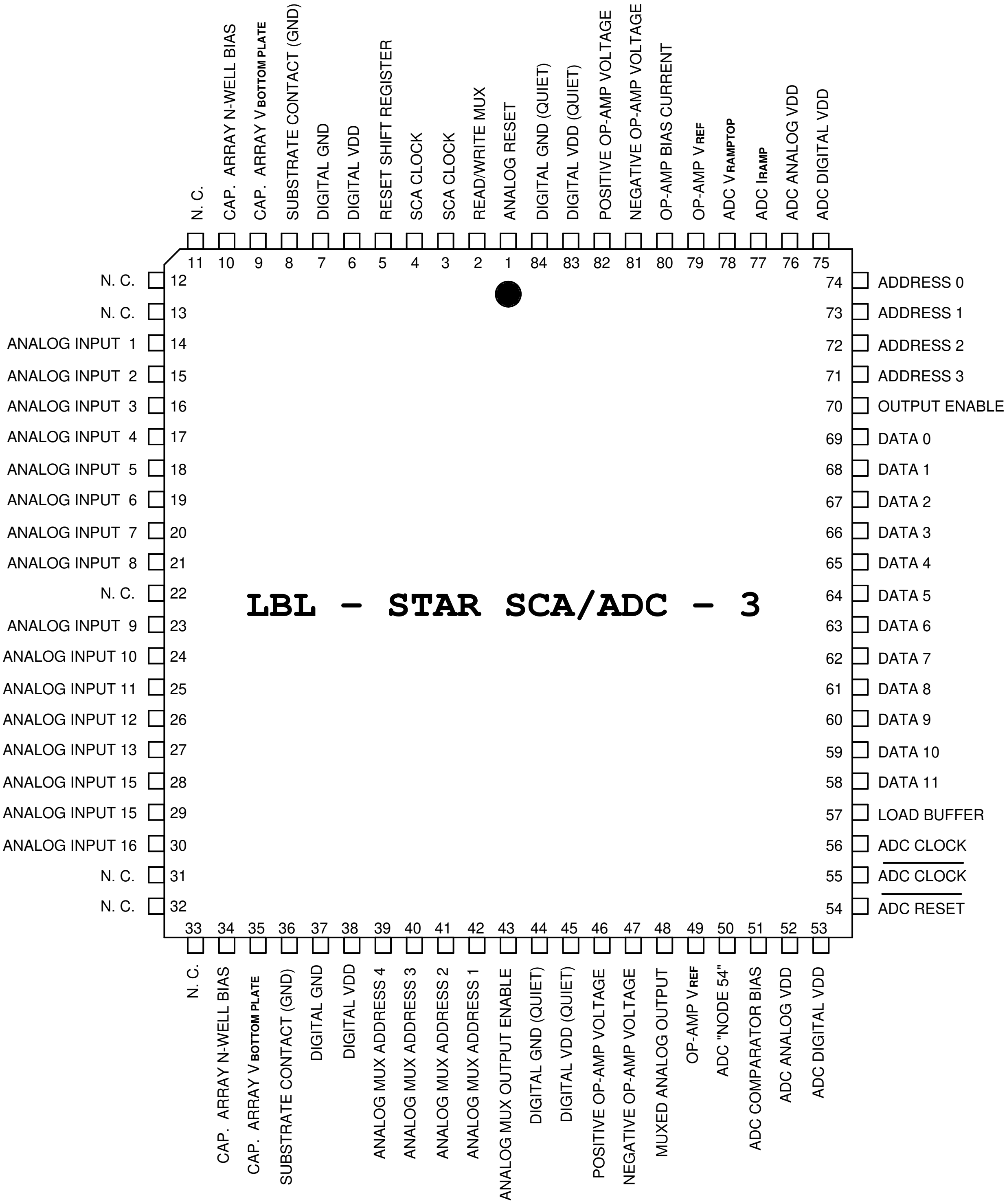
Pin Configuration



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Absolute Maximum Ratings

$V_{DIGITAL}$ to GND .... -0.3V to +7V
V_{ANALOG} to GND .... -0.3V to +7V
$V_{IN[N]}$ (analog) to GND........ -0.3V to +7V
Digital Inputs .... -0.3V to +7V
Operating Temp................. TBD
Storage Temp .... -65°C to 70°C
Power Dissipation .... TBD

Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		4.75	5.0	5.25	Volts
Analog Supply Current	I_{DD}	SCA/ADC Quiescent SCA/ADC Active		16 16	20 20	mA
Digital Supply Voltage	V_{CC}		4.75	5.0	5.25	Volts
Digital Supply Current	I_{CC}	SCA/ADC Quiescent SCA/ADC Active	2 2	3 4.6	6 9	mA
Power Dissipation		SCA/ADC Quiescent SCA/ADC Active	50 50	95 103	130 145	mW
ANALOG INPUT						
Input Voltage Range	V_{INX}		0	1.6 to 3.4	5.0	Volts
Input Impedance				8KΩ || 22pf		
ANALOG OUTPUT						
Analog Mux Output	V_{OUTX}		0	1.6 to 3.4	5.0	Volts
Device Gain			-0.85	-0.9	-0.95	V/V
DIGITAL INPUT						
High Level Input Voltage		CMOS Compatible	V_{CC}-0.5	V_{CC}	V_{CC}+0.5	Volts
Low Level Input Voltage		CMOS Compatible	-0.5	0	+0.5	Volts
ADC Clock Frequency	f_{CLOCK}			25		MHz
ADC Clock Duty Cycle			40%	50%	60%	
DIGITAL OUTPUT						
Output High Voltage	V_{OH}	V_{OH} @ I_{OH} = 1mA	V_{CC}-0.5		V_{CC}	Volts
Output High Current	I_{OH}	I_{OH} @ V_{OH} = V_{CC}-0.5 V	1			mA
Output Low Voltage	V_{OL}	V_{OL} @ I_{OL} = 4mA	0.0		0.5	Volts
Output Low Current	I_{OL}	V_{OL} @ I_{OL} = 0.5 V	4			mA