Front-End Electronics => DAQ Fiber Interface

Requirement Document

Version 1.2 - April 10, 1996

V. Lindenstruth, R. Bellwied, F. Bieser, B. Bonner, M. Botlo, J. Cannon, H. Crawford, L. Greiner, G. Hoffmann, R. Jared, S. Klein, M. LeVine, T. Noggle, J. Schambach, D. Underwood

Sign-Off Page

The STAR management and group leaders agree to the definition of the interface defined in this document. Further changes to this interface will require the written agreement of all involved parties.

Jay Marx

Richard Jared

Rene Bellwied

Fred Bieser

Billy Bonner

Tom Cormier

Henry Crawford

Volker Eckhardt

Spencer Klein

Mike LeVine

Change Log

November 94	V1.0	First version accepted
September 95	V1.0a	Fiber commands clarified
April 96	V1.1	Document converted to FrameMaker, SVT and TPC specific updates, geometry changed according to STAR note #229

1. Introduction

This document describes the fiber optic interface between the front-end electronics on the detector and DAQ in the counting house. The front-end of the detectors is implemented on readout boards on the detector. The DAQ front end will be in the counting house receiving the raw data through fiber links. Chapter 2 of this document describes the requirements for the discussed interface for the various detectors. Chapter 3 defines the implementation in sufficient detail so that all involved groups can design their part of the interface with the guarantee that these interfaces will properly interact.

The highest demands with respect to optical data transmission are imposed by the TPC and SVT detectors. The data rate requirements of both the TPC and SVT are met by the specifications of the HP Gigalink chip set (HDMP-1012/1014), which allows transmission of 20-bit words at a word rate of up to 62.5MHz. There will be two 10-bit ADC values of two different channels sent simultaneously to fully utilize the 20-bit transmission. There are appropriate optical receivers and transmitters available that allow a fiber based data transmission over a long distance and completely ground-loop-free data connection between the detector and the counting house. It has been agreed upon to use these or compatible devices supporting the 24-bit CIMT[1] encoding as the physical interface between the readout boards on the detector and the DAQ front-end, which are called receiver boards.

Figure 1 (left) shows a sketch of the fiber connection between the front-end readout cards and the DAQ receiver boards. Note that the busy return signals are represented in a logical way. The right side of the figure shows the format of the data transmission. There has to be some maintenance information about the given event that will be encapsulated into a header. The actual raw data follows that header. Header and data can be disentangled by command words. During the data transmission abort commands may be transmitted.

1. Conditional Invert Master Transition

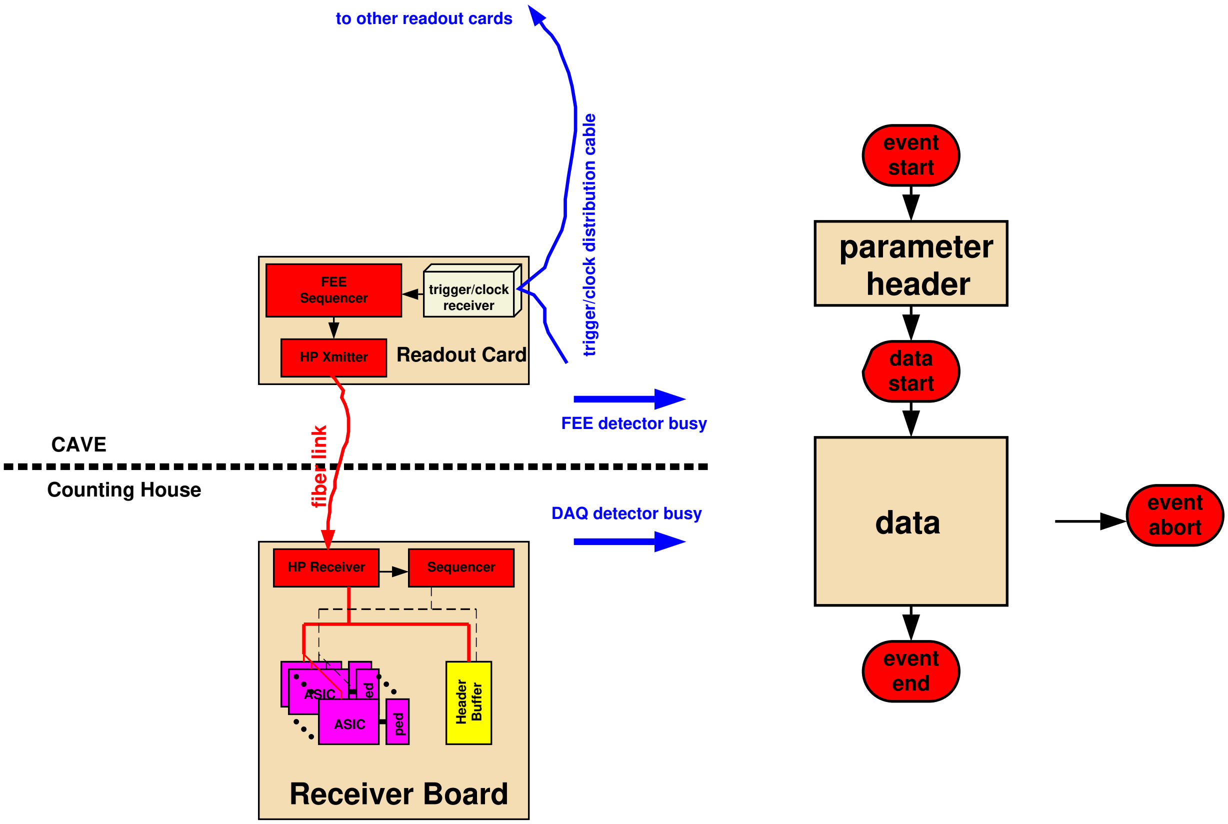


FIGURE 1: *Left: A sketch of the interface between the front-end readout cards and the DAQ TPC receiver boards.*
Right: A sketch of the data format. The two data sections are encapsulated by command words.

2. Requirements

2.1 Bandwidth

Requirement

Support enough bandwidth to send the uncompressed 10-bit raw data of both the TPC readout board pair and the SVT readout board within 10 ms to the DAQ receiver boards in the counting house.

Justification

The transmission speed defines the dead time per event and consequently the detector performance. The TPC and SVT digitization time is 10 ms. The time allowed for transmission of a TOF, EMC or ShowerMax event is not finalized yet. The uncompressed raw data volume of one Au+Au event is listed below:

TPC: (36 FEE cards per readout board pair) * (32 channels per FEE card) *
(1024 time buckets per channel) * (10-bit ADC value per time bucket) =
$1.18*10^6$ words(10-bit)

SVT: (18 Si detector halves per readout board) * (256 channels per detector half) *
(128 time buckets per channel) * (10-bit ADC value per time bucket) =
$0.553 \bullet 10^6$ words(10-bit)

TOF: (60 channels per tray) * (120 trays) * (10-bit ADC, 12-bit TDC per ch.) =
$14.4*10^3$ words(12-bit)

EMC: (4800+1440 channels) * (16-bit ADC value per channel) =
$6.24*10^3$ words(16-bit)

ShowerMax:(32000+7500 channels) * (10-bit ADC value per time bucket) =
$3.95*10^4$ words(8-bit)

XTPC: The XTPC electronics is not defined yet but it is likely that the TPC electronics will be used.

Note:
Each SVT detector half has 240 channels. However, to ensure compatibility with the cluster finder ASIC which requires either 64 or 256 channels, 16 padding channels will have to be sent for each time bucket.

The ShowerMax will perform zero suppression in the front-end. Correspondingly, the raw data volume numbers quoted here define an absolute maximum per event.

The ShowerMax detector has a 14-bit dynamic range but needs only 8-bit resolution. Consequently the 10-bit value will be translated into 8-bits as in case of the TPC and SVT.

The ShowerMax event size will vary since the L1 processors will sparsify the ShowerMax raw data before it will be sent to DAQ. The numbers stated above are correspondingly an upper limit. There will be a small overhead for the compressed data format.

The actual number of ShowerMax channels is uncertain.

2.2 Fiber Commands

Requirement

The fiber link has to support the command sequence as sketched in Figure 1 (left) and the command codes listed in Table 1 on page 7.

Justification

The ability to interrupt the transmission of the raw data at any time in case of a L1/L2 abort is required.

Encapsulation of the header and data phase with command words to ensure data integrity and to steer the sequencer on the receiving end of the fiber link is very useful.

Note: These command words are only intended to control the sequencer on the receiver board. They will not support any command transmission from the readout board/trigger system to DAQ. The trigger command and DAQ command will be part of the header.

Currently each command will be followed by the appropriate number of idles to make up for about 100 ns of wait states.

The command sequence for the case of two aborted events followed by an accepted event is: 1,2,8,1,2,8,1,2,4.

For debugging purposes all front-end boards will hold-off with the transmission of the end-event command until a L2 accept or abort has been received. This will prevent DAQ from processing the given event until the L2 decision (accept or abort) has been derived.

TABLE 1. *The fiber command codes*

event-start	(cmd=0x01):	This command starts the sequencer on the receiver boards. It will configure itself to be ready to accept the header data.
data-start	(cmd=0x02):	This command precedes the transmission of the raw data. If the sequencer on the receiver board detects this command before it receives exactly 64 header words, it will flag an appropriate sequencing error bit. During the raw data phase, event-abort commands are possible at any time.
event-end	(cmd=0x04):	This command defines the normal and complete transmission of an event. If the internal counters of the sequencer on the receiver board do not indicate that all header or data words have been received, then appropriate error bits have to be set indicating this sequencing error. Upon receipt of this command, the receiver boards will be busy for about 400 µs. After that time, the DAQ front-end busy will be released if there is at least another buffer available.
event-abort	(cmd=0x08):	An event may be aborted any time during the data phase. This command will be used for the SVT and TPC data transmission.

2.3 Header

Requirement

Send fixed-length header information preceding the data, such as the trigger/DAQ command, trigger token and status of the readout board, including local bunch crossing counters and geographic readout unit IDs. The length of the header is fixed for any detector and cannot exceed 512 bytes. The first 16 words of the parameter header must comply with the format shown in Figure 2.

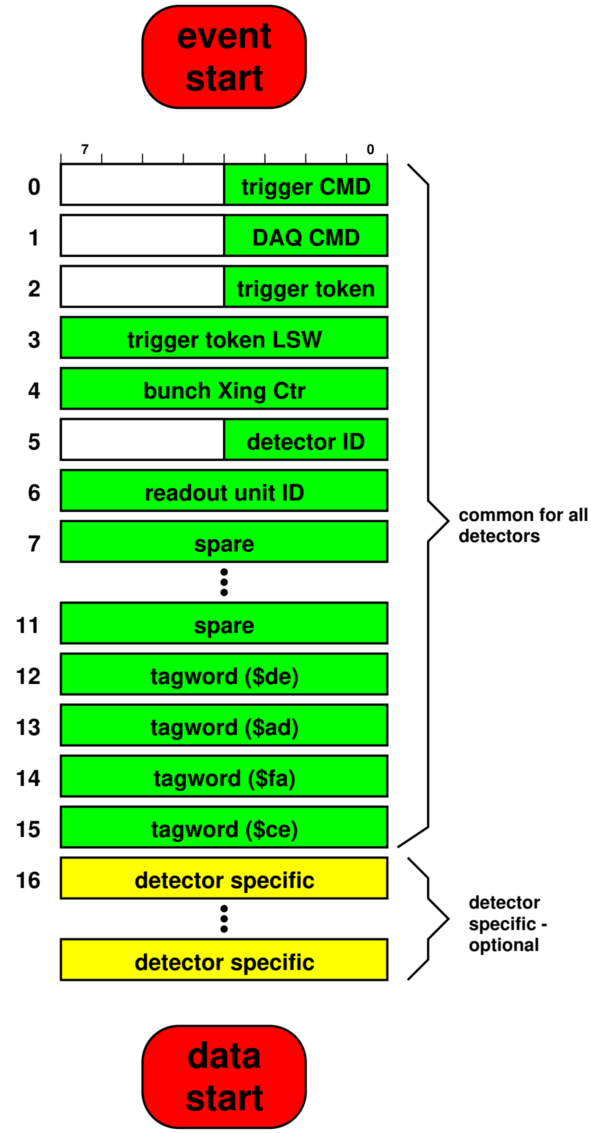
Insert wait states depending on word clock rate to limit header word cycle time to a minimum of 30 ns (refer to 2.7 on page 11).

Justification

ID and maintenance information is required to accompany the raw data to allow identification of which detector and event the given buffer belongs. The trigger system will send a trigger command and a unique trigger token to each individual readout board. All readout boards will have a unique geographic ID that they send in the header together with the raw data. The readout boards will also count the bunch crossing number. This counter will ensure the integrity of the trigger distribution cabling.

FIGURE 2: *The layout of the parameter header. The four tag words are implemented to have a redundancy check for correct header transfer.*
The number of valid bits in the readout unit ID field depends on the detector specified in the detector ID. Any unsignificant leading bits have to be forced to zero in this data word.
The number of significant board ID bits are:

TPC:	*8*
SVT:	*5*
TOF:	*7*
EMC:	*7 (estimated)*
ShowerMax:	*6 (estimated)*



DAQ needs some handling information about the raw data buffer that may select different options in the code of the front end processors or L3. This information is distributed through the trigger tree together with the trigger command to all readout boards. They will forward that command to DAQ in the parameter header.

Currently there are two definitions for the detector specific data fields. The first two words of the TPC detector specific header (word 16 and 17) shall define 16-bits of prom ID uniquely identifying the prom version of the FPGA source prom on the readout board. The SVT will send an SCA offset count in word 16 and a 16-bit program ID (identifying the program version of the PLD source code on the readout board) in words 17 and 18.

Other detectors may omit the detector specific data phase.

The header data may be stored in some extra memory or FiFo. To reduce the implementation costs the cycle time of this header memory is defined not to exceed 30 ns. This will require one wait state for the TPC and

SVT links running at about 60 MHz word rate (1.5 GBits/sec bit rate). Wait states may not be required if the fiber link is running at slower bit rates.

TABLE 2. *The definition of the detector ID field in the header*

detector	detector ID
TPC	1
SVT	2
TOF	3
EMC	4
ShowerMax	5
XTPC	6

2.4 Configuration Events

Requirement

Support configuration events that define the mapping between physical detector channels, such as TPC pad and padrow numbers and channels of the detector-daq interface. For SVT and TPC, only the lower 8 of the 10 data bits of each channel (high and low word of the 20-bit HP data bus) shall be valid during configuration events. The number of words transferred in the case of configuration events has to be exactly the same as in the case of the transmission of raw data.

Justification

The concrete order of the channels transferred is detector specific. The mapping of channels of the readout board onto the TPC pad and padrow numbers, depends on the geometric position of the readout board. However, this mapping will be fixed.

In order to determine the channel mapping, there will be special data formats responding to housekeeping triggers like the geographic readout. These events will contain ID information instead of raw data. This ID information defines which detector channels (i.e., pad and padrow number) are mapped onto a given channel in the receiver board.

TPC and SVT raw data events comprise two 10-bit ADC values per 20-bit word. In the case of configuration events, only the lower 8-bits of the 10-bit word will be used. This restriction is required because TPC and SVT configuration events will be sent through the ASICs without pedestal correction and gain mapping. The back end bus of the ASIC is only 8-bits wide allowing the storage of only 8-bit values.

The number of words transmitted for configuration events will not differ from raw data to allow the same sequencer logic to handle both events. There are 1024 configuration bytes (8-bit) per TPC pad in the case of a TPC configuration event and 128 per SDD anode in the case of an SVT configuration event. It is expected that only a very small fraction of that will be used.

2.5 Aborts

Requirement

❶ Support aborts during the data transmission of *slow* detectors such as TPC, SVT and XTPC due to aborts issued by the trigger system. These aborts are forwarded to DAQ on the fiber link.

❷ *Fast* detectors like TOF and EMC cannot abort an event once it is transmitted to DAQ. They have to hold on to an event until they receive a L2 accept from Trigger.

Justification

The trigger system may issue L1/L2 aborts any time up to 5 ms after a trigger command. There are two kinds of detectors in STAR: *slow* detectors such as TPC, SVT and XTPC (readout time about 5 ms) and fast detectors such as EMC and TOF.

Because the TPC and SVT readout boards will be located on the detector and hard to access and maintain, they shall be kept as simple as possible. There will be no elasticity buffers on the readout boards. They will send the data synchronously to the DAQ receiver boards as it is digitized using a state machine that is started with an incoming trigger request. Consequently aborts will have to be forwarded to the DAQ receiver boards. They can happen any time between the *data start* and *data end* commands (refer to Figure 9).

For fast detectors, aborts may happen after events have been completely readout. In order to simplify the interface between the front-end and DAQ, the second requirement is imposed. This scenario requires the buffer clear logic to reside on the detector. Each event will be sent through the fiber to DAQ only if it is certain that this event will not be aborted – upon receipt of a L2 accept. There is, however, enough elasticity buffer space required to buffer raw data for up to 5 ms assuming maximum L0 trigger rate. However, both EMC and TOF events are fairly small, and this buffer requirement does not require much memory.

2.6 ASIC Compatibility

Requirement

The TPC and SVT raw data format has to be compatible with the final STAR ASIC implementation version 4.2 December 2, 1994.

Justification

The design of the STAR cluster-finder ASIC requires all channels of a given time bucket to arrive before the first channel of the next time bucket can be accepted. The number of channels per ASIC is fixed – 64 for the TPC mode and 256 for the SVT mode.

This requirement deals with the internal sequencer in the ASIC. Essentially, there is one slow running global time counter and a fast running channel counter. Every time the channel counter wraps, the time counter is incremented. Correspondingly, the readout board has to send to all channels of a given time bucket before it can advance to digitize the next time bucket.

The ASIC does not have any elasticity input buffers. Therefore, it has to receive a data word every 150 ns in order to achieve 10 ms dead time (e.g. TPC: 1024 pixels times 64 channels per 10 ms). It cannot accept data at shorter time intervals than 150 ns. Strobing it slower would result in a dead time greater than 10 ms per event.

The parameter data mentioned in 2.2 on page 6 will bypass the ASIC.

All front-end electronics boards are required to send the same number of data words. Readout boards with fewer FEE channels shall zero fill the unused data channels. This allows one generic sequencer at both the readout and the receiver board.

In case of configuration events (trigger command 12...15), the TPC and SVT raw data is restricted to having only 8 valid bits, because the buffers at the back-end of the ASIC are only 8-bits wide. Data words wider than 8-bits have to be split into several words. In order to use the same sequencer logic for raw data and configuration data, the configuration events shall have exactly the same size as a normal event. Therefore, there are 1024 bytes of configuration data per TPC channel and 128 bytes of configuration data per SVT channel

2.7 Wait States

Requirement

Allow to insert padding or idle words after each command word and header word.

Allow to insert padding or idle words after each header word in order to limit the header word rate (refer to 2.3 on page 7).

Justification

Both the sequencer on the readout and the receiver boards need certain time to react to the various state changes of the system. For example, it may be required to delay the transmission of raw data after the parameter headers to give the sequencer on the DAQ receiver boards time to reconfigure for the data mode. The interface definition has to be able to accommodate this requirement.

Note: Currently, each command will be followed by the appropriate number of idles to make up for about 100 ns of wait states.

After each header data word, there has to be one wait state in the TPC and SVT link to accommodate slow header buffers at the receiving end. Depending upon the fiber speed, header wait states may not be required for EMC and TOF.

2.8 Variable Channel Count

Requirement

The number of raw data channels transferred from any TPC/SVT readout board of a given detector has to be fixed.

Other detectors may transmit variable length events.

Justification

Some TPC readout boards will not have the full number of channels (36 FEE cards for the TPC) attached to them. Due to the layout of the detector, there may also be blind channels. However all readout boards will send data as outlined in 2.1 on page 5. The appropriate unused slots in the transmission sequence shall be filled with zeroes. (This is not a strong requirement because the front end processors can be programmed to ignore certain channels depending on some mapping that will be downloaded during the configuration phase.) This requirement for SVT and TPC allows exactly the same sequencer logic for both detectors on both the readout boards and receiver boards.

Other detectors may transmit sparsified data to DAQ.

3. Data Formats

3.1 TPC

The DAQ requirement for the sequencing of the TPC channels is that as many as possible complete padrows should be sent to one mezzanine board. This minimizes the number of potential cases where fractions of one cluster end up on more than one mezzanine board. This requirement is most important for the outer sector.

Figure 3 shows the pad and FEE connector layout of the outer sector. There is one receiver board for eight padrows and four receiver boards for the whole outer sector. The sequencing will be defined for the eight outer padrows. The same sequencing will be implemented for all other padrows.

The ideal mapping of pads onto the three mezzanine boards of one receiver board is pad number 1...384 going to mezzanine board A, pad number 385...768 going to mezzanine board B and pad number 769...1152 going to mezzanine board C. In this scenario only the minimum of two padrows would not be completely sent to one mezzanine board.

The over all sequence of data words is similar to the TPC setup:

time bucket (0 ... 1023)
FEE A/B channel (0 ... 15)
FEE A/B card (36 FEE cards)

The sequence of FEE cards is outlined in Table 3 and Table 4. Each FEE card reads pads from two padrows. With respect to Figure 3, the upper padrow of one FEE card is labelled A and the lower B. The group of 16 pads of the upper padrow of the first FEE card in the upper left corner of Figure 3 would be labelled 0A.

Exactly the same sequence of FEE cards will be used for all other groups of 8 padrows. Because the number of pads per padrow and the number of FEE cards changes as one moves more towards the inner end of the outer sector, some FEE card slots will be left empty and will be filled with zeroes. Table 4 shows how the FEE cards of the inner readout boards are mapped with respect to the outer readout/receiver board.

STAR Outer Sector Prototype Pad Plane

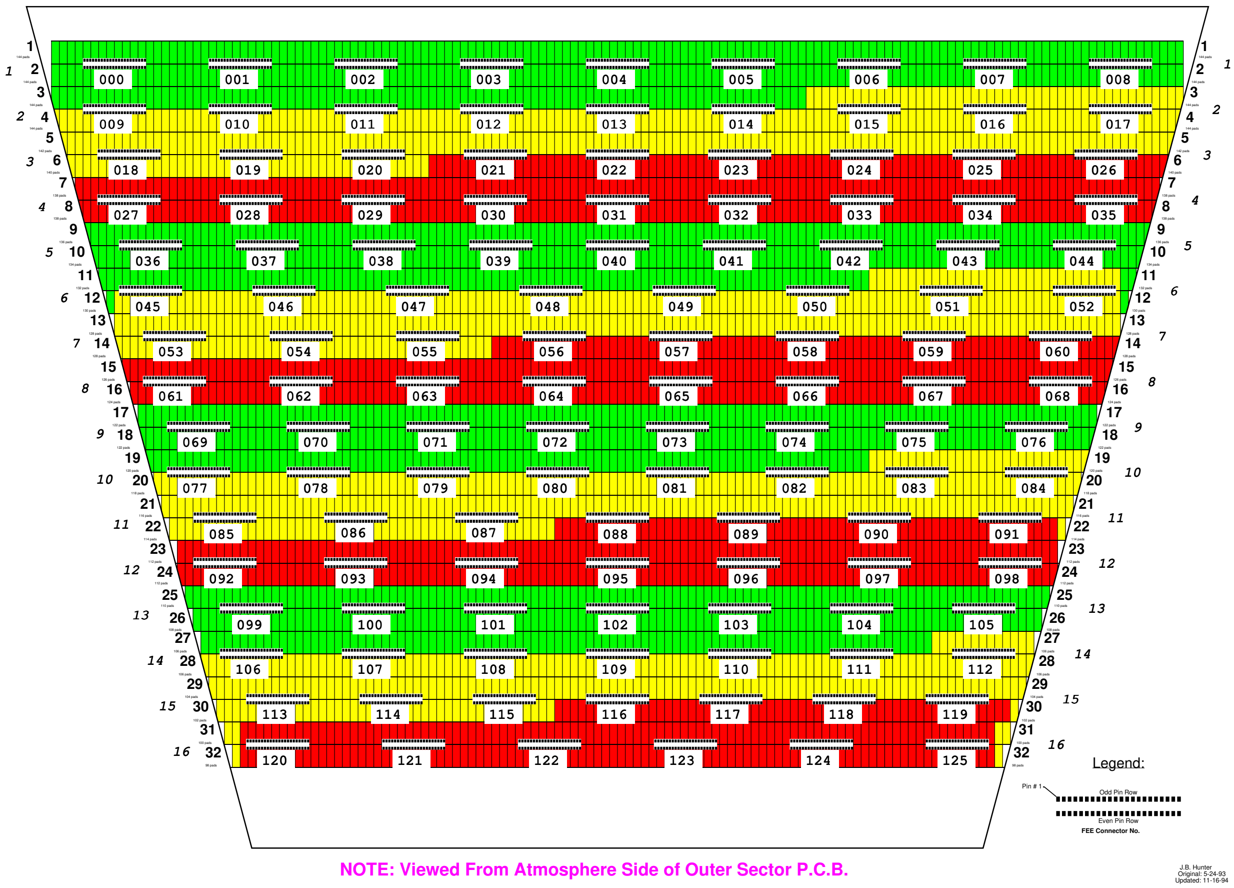


FIGURE 3: *A sketch of an outer TPC sector. Eight padrows are multiplexed into one fiber/receiver board. There are 4 receiver boards per outer sector. All pads that will end on one mezzanine of one receiver board are labelled with one color or grey scale. There are four groups of padrows with the same color or grey scale. There will be four receiver boards for the outer sector.*

TABLE 3. *Sequence of FEE A/B groups for a given time bucket and A/B channel*

sequence number	mezz A		mezz B		mezz C	
	H	L	H	L	H	L
0	00A	01A				
1	02A	03A				
2	04A	05A				
3			15A	16A		
4			17A	09B		
5			10B	11B		
6					21B	22B
7					23B	24B
8					25B	26B
9	06A	07A				
10	08A	00B				
11	01B	02B				
12			12B	13B		
13			14B	15B		
14			16B	17B		
15					27A	28A
16					29A	30A
17					31A	32A
18	03B	04B				
19	05B	06B				
20	07B	08B				
21			18A	19A		
22			20A	21A		
23			22A	23A		
24					33A	34A
25					35A	27B
26					28B	29B
27	09A	10A				
28	11A	12A				
29	13A	14A				
30			24A	25A		
31			26A	18B		
32			19B	20B		
33					30B	31B
34					32B	33B
35					34B	35B

TABLE 4. *The sequence of FEE cards of the other receiver boards of the outer sector with respect to board 1*

receiver bd 1 FEE card #	receiver bd 2 FEE card #	receiver bd 3 FEE card #	receiver bd 4 FEE card #
0	36	69	99
1	37	70	100
2	38	71	101
3	39	72	102
4	40	73	103
5	41	74	104
6	42	75	105
7	43	76	--
8	44	--	--
9	45	77	106
10	46	78	107
11	47	79	108
12	48	80	109
13	49	81	110
14	50	82	111
15	51	83	112
16	52	84	--
17	--	--	--
18	53	85	113
19	54	86	114
20	55	87	115
21	56	88	116
22	57	89	117
23	58	90	118
24	59	91	119
25	60	--	--
26	--	--	--
27	61	92	120
28	62	93	121
29	63	94	122
30	64	95	123
31	65	96	124
32	66	97	125
33	67	98	--
34	68	--	--
35	--	--	--

3.2 SVT

Each SVT detector has two hybrids on its two opposite sides with 240 channels each. The sequence of SVT raw data channels is relatively unconstrained since one SVT hybrid maps directly onto one ASIC (the upper 16 channels are filled with padding zeroes). Unlike the TPC system, there are no clusters overlapping between detectors/ASICs. It is relatively irrelevant which detector is mapped onto which ASIC or mezzanine board of the DAQ receiver board. Figure 4 shows a sketch of the SVT detector. Each box represents one detector with two hybrids. The whole detector can be split into octants, four quadrants on each side. Each octant is sending uncompressed raw data through three fibers. The grouping is indicated by different colors in Figure 4. Each group consists of 9 silicon detectors or 18 hybrids. Two of the three groups have the same mapping (group 1 and 2). They are shifted by $\pi/4$ in Φ. Due to the implementation constraints of the ASIC (refer to 2.6 on page 10), the overall order of raw channels is defined as follows:

time bucket (0 ... 127)
detector channel (1 ... 240, 16 padding zeroes)
detector hybrid(18 hybrids as listed in Table 3)

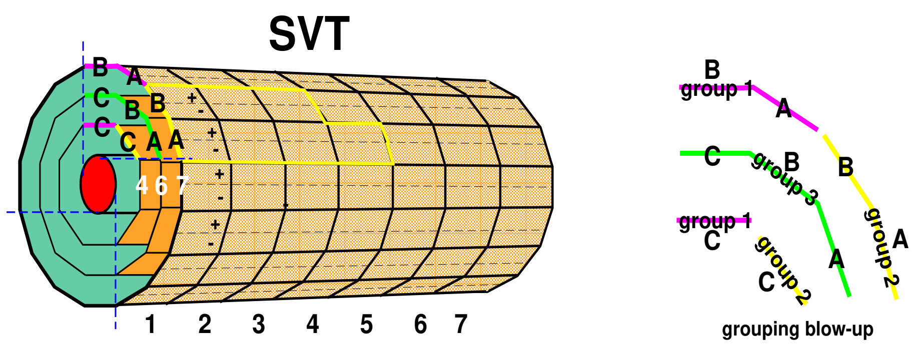


FIGURE 4: *A sketch of the SVT detector geometry. There are three fiber links per octant as indicated with different colors.*
Note: Each box in this figure represents a full detector with two detector elements which are read out separately.

There are 18 hybrids sent per detector channel as indicated in the table above or 256 detector channels (including padding zeroes) times 18 hybrids per time bucket. The hybrid number index is running the fastest.

The 18 hybrids in the two groups are assembled as follows: In group 1 ladder A contributes 8, ladder B 6, and ladder C 4 hybrids. In group 2 all three ladders contribute 6 hybrids each. The boundaries of these contributions are indicated by different colors in Figure 4. The 18 hybrids in each group are connected to 3 ADC's each on the readout system. The sequencing of the ADC values for each hybrid onto the fiber link is fixed and is shown in Table 5. The notation used in this table is as follows: **h**n = hybrid n (n=1,18, corresponding to 18 detector halves), **c**n = channel (anode) n (n=1,256), **t**n = time bucket n (n=0,127). The "-" indicates 10-bit ADC values that are combined to 20-bit fiber link words.

TABLE 5. *The SVT hybrid sequence for one channel and one time bucket*

Sequence Number	High	-	Low
0	h1c1t0	-	h2c1t0
1	h3c1t0	-	h4c1t0
2	h5c1t0	-	h6c1t0
3	h7c1t0	-	h8c1t0
4	h9c1t0	-	h10c1t0
5	h11c1t0	-	h12c1t0
6	h13c1t0	-	h14c1t0
7	h15c1t0	-	h16c1t0
8	h17c1t0	-	h18c1t0

... (vary channel number with same 9 sequences, then vary time bucket number)

One mezzanine would have as much overlap as possible in η/Φ space.

4. Readout Unit IDs

4.1 TPC board IDs

The TPC has a total of 144 readout boards, 6 per sector. Figure 5 shows a sketch of the position of the TPC readout boards in the TPC wheel. The big numbers in Figure 5 define the TPC sector number as seen from the outside of the magnet. The readout boards are numbered sequentially from outside to inside starting at 1. Pad number 1 of the outer sector is read out by the TPC readout unit number 1.

FIGURE 5: *The position and number of the TPC readout boards on the TPC pad plane and the numbering scheme of the TPC sectors in the TPC wheel as seen from the west end (z>0) looking toward the interaction region. The sector numbers on the east end (z<0) are similarly arranged with numbers counting from 13 to 24.*

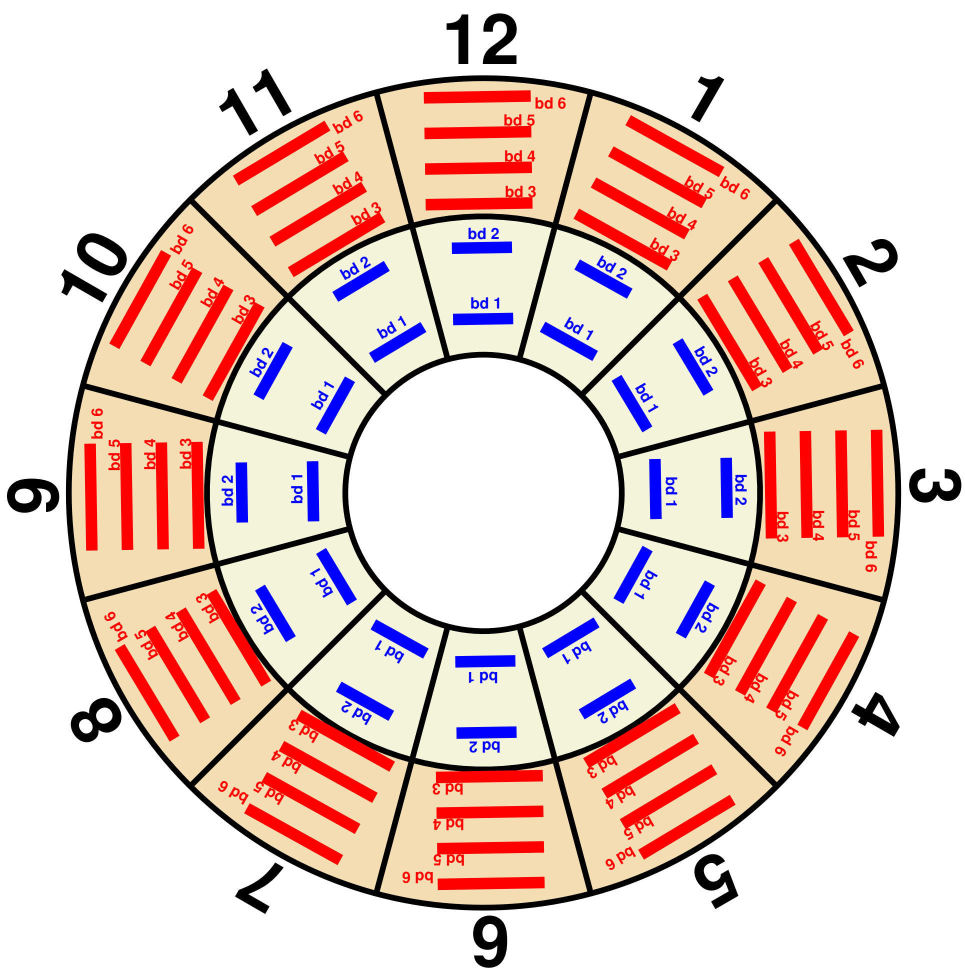
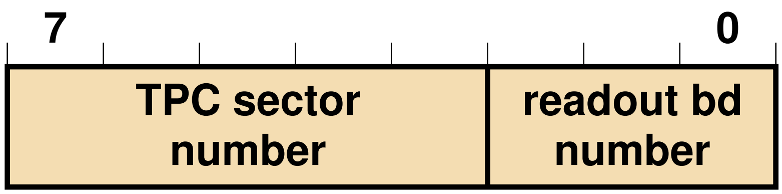


Figure 6 shows the corresponding TPC readout unit ID definition.

FIGURE 6: *The definition of the 8-bit readout board ID.*



4.2 SVT board IDs

The SVT has a total of 24 readout boards, 12 on each side of the STAR detector. Figure 7 shows a sketch of the position of the 12 SVT readout boards in the TPC wheel. There will be one SVT readout board per TPC sector. Which SVT detectors a given readout board in the TPC wheel reads is also indicated in Figure 7. The same nomenclature is used as in Figure 4. The TPC sector numbers are defined as seen from the outside of the magnet. Group 1 in Figure 4 is SVT readout unit ID 1, group 2 ID 2, and group 3 corresponds to readout unit ID 3.

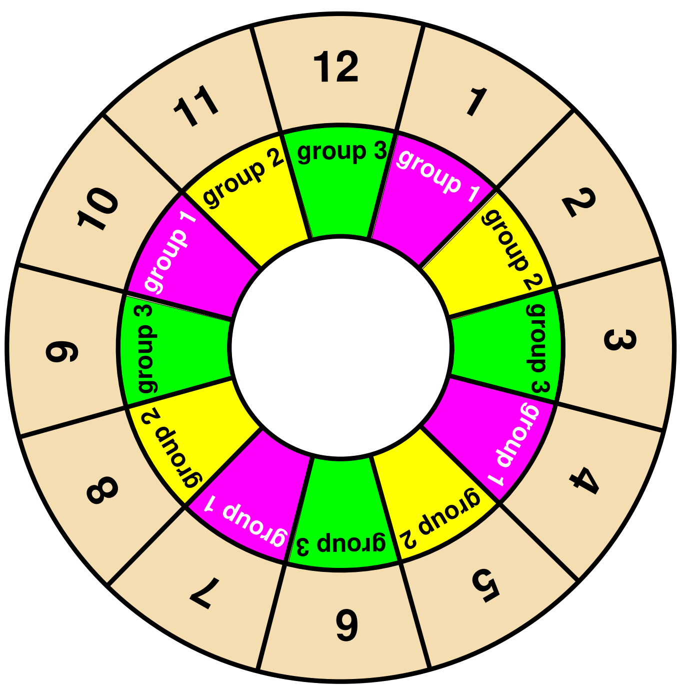


FIGURE 7: *The position and read out sequence of the SVT readout boards in the TPC sector wheel as seen from the west end (z>0) looking toward the interaction region. The readout board numbers on the east end (z<0) are similarly arranged, with numbers counting from 13 to 24.*

Figure 8 shows the corresponding SVT readout unit ID definition. The SVT readout boards are numbered with respect to the corresponding TPC sector number from 1 to 24.

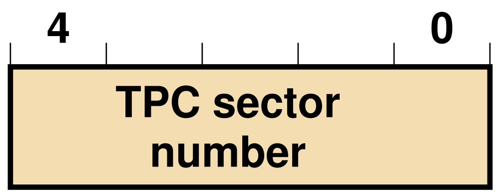


FIGURE 8: *The definition of the 5-bit SVT readout board ID.*

5. Implementation

Figure 9 shows a sketch of the data flow from the readout boards to the DAQ receiver boards as an example for the TPC or SVT. There are two data phases: header and data. Both the header and data phase are encapsulated by command words. The HP transmitters allow to disentangle command words from data words (/DAV, /CAV in- and outputs). The command strobes are used to transfer the command words. After each command strobe the sending readout board will insert a constant wait state of about 100 ns (6 transmission clocks). This can be accomplished by not strobing either /DAV or /CAV.

The headers are fixed length and 8-bits wide. The first 16 bytes of the header are common for all detectors. The rest of the header (48 bytes in case of TPC and SVT) is free to be defined detector specific. Figure 2 (Section 2.3) defines the header format. Note that the width of the board ID depends on the detector.

TPC and SVT raw data events consist of two 10-bit ADC values per 20-bit word. In the case of configuration events, only the lower 8-bits of the 10-bit word will be used. This restriction is required because configuration events shall be sent through the ASICs with pedestal correction and gain mapping switched off. The back end bus of the ASIC is only 8-bits wide allowing to store only 8-bit values.

The data of other detectors may be sparsified before it is sent to DAQ. This interface accommodates this requirement. Between the *data start* and *event end* commands, any number of words may be transmitted.

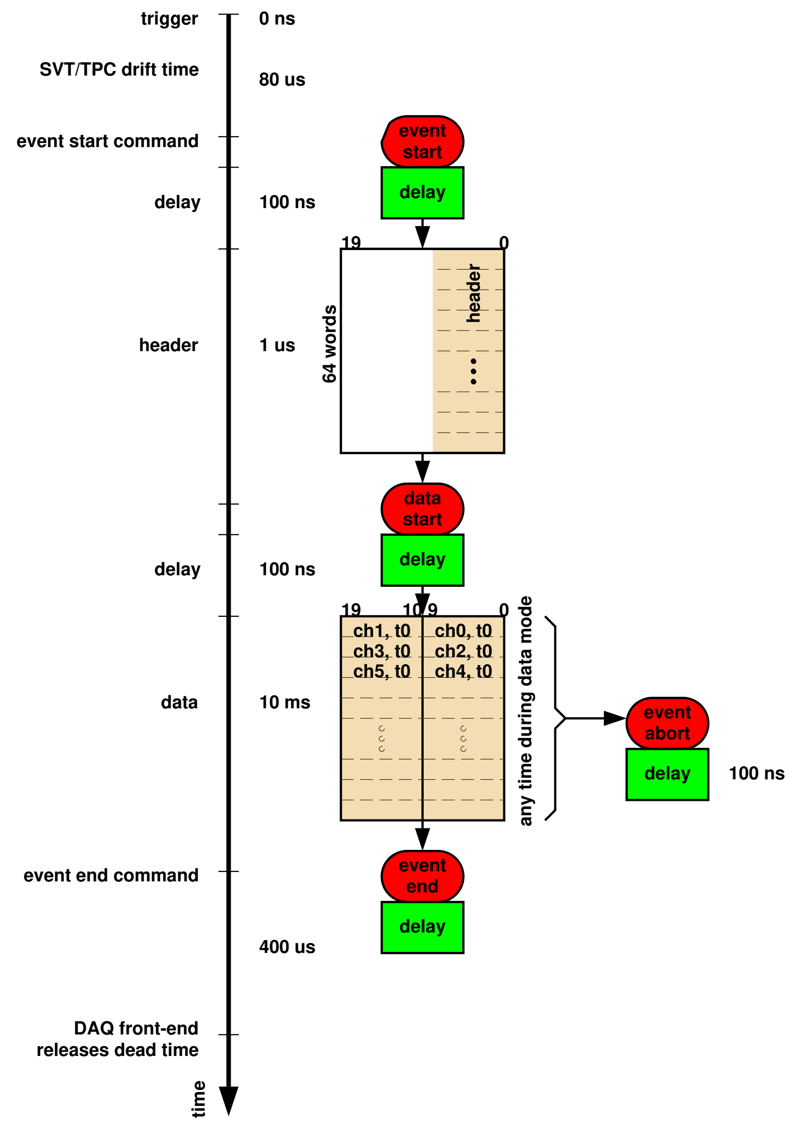


FIGURE 9: *The dataflow through the fibers using the TPC or SVT scenario as an example. The 400 µs time after the event end command is used by the DAQ front-end to readout the cluster pointers of the ASIC and to release the dead time if more buffer space is required.*