Tests Août 2004

Avant installation définitive

Avec Slow Control Epics + Minidaq LabView

Pas de polarisation HT – Une seule face lue à la fois.

Notation : Hxx means Hybrid xx

Cxx means Costar of hybrid xx

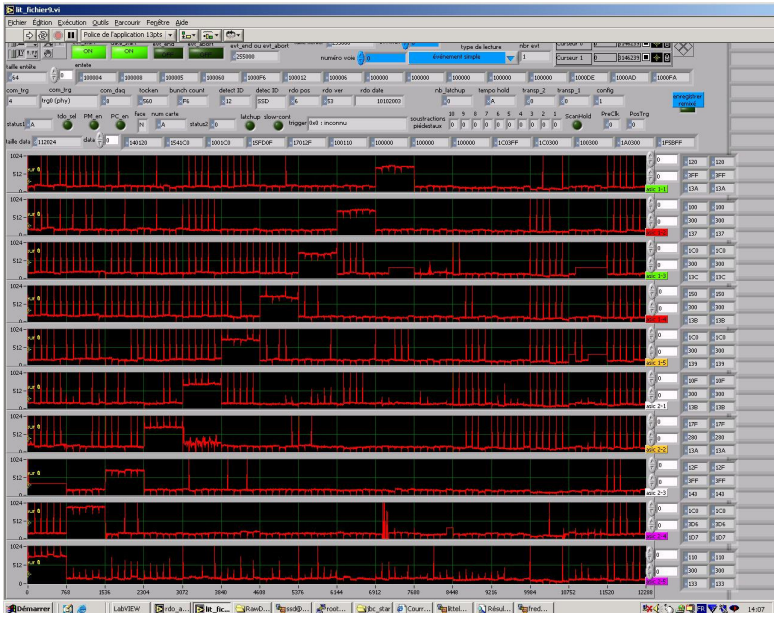
Axx means A128C xx on a given hybrid.

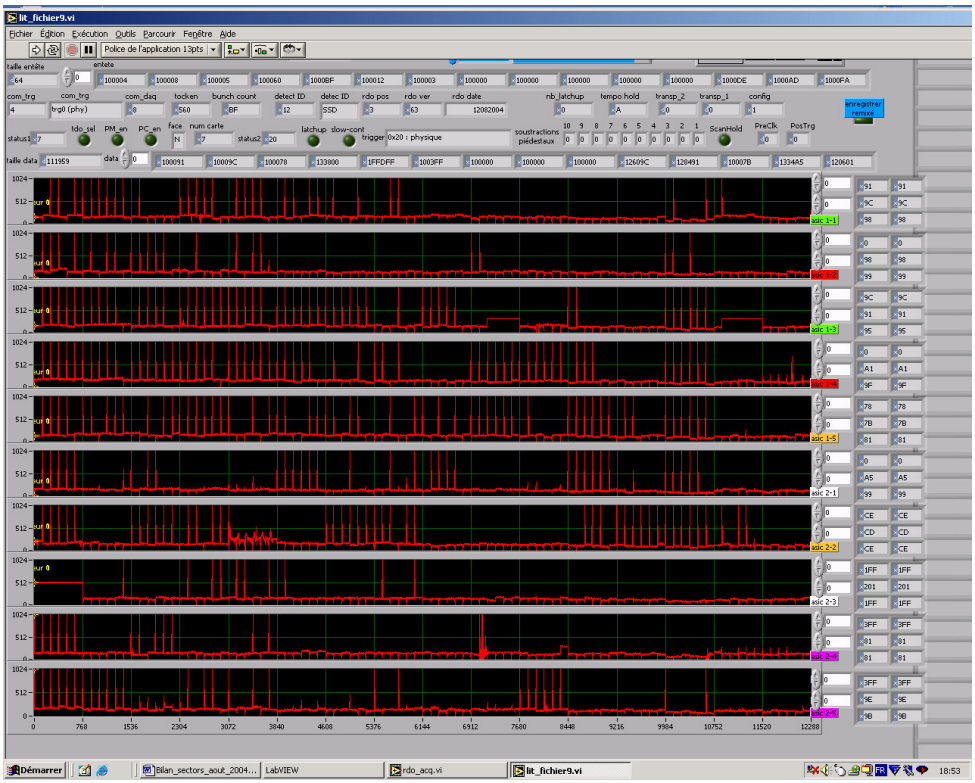
Correction of the pedestal offset by the readout board :

Word in the Slow control	0	1	2	3	4	5	6	7	8	9
Ladder	2	4	1	6	3	8	5	10	7	9
	19	17	20	15	18	13	16	11	14	12

Adresse hexa	Adresse binaire	Ladders sur RDO 1N	Ladders sur RDO 1P	Ladders sur RDO 2N	Ladders sur RDO 2P
2	0010	10N	10P	11N	11P
6	0110	8N	8P	13N	13P
7	0111	6N	6P	15N	15P
5	0101	4N	4P	17N	17P
4	0100	2N	2P	19N	19P
C	1100	1N	1P	20N	20P
D	1101	3N	3P	18N	18P
F	1111	5N	5P	16N	16P
E	1110	7N	7P	14N	14P
A	1010	9N	9P	12N	12P

Sector 1N (ladder 1N to 10N)





I. LADDER 1 (LAD03 - Ancienne spare)

No problem. C9 to C16 bypassed.

II. LADDER 02 (LAD09)

No big problem. A noisy area on H10. A6 missing on H11. Still missing when the bias parameters are modified.

III. LADDER 03 (LAD24)

C1 bypassed. H1 missing. Everything else OK. H1 still missing even with the force bias.

IV. LADDER 04 (LAD17)

H1 with a noisy area. H5 has a very bad pedestal. C5, C10 and C16 bypassed.

V. LADDER 05 (LAD12)

Everything OK.

VI. LADDER 06 (LAD18)

Everything OK except H15 with some missing chip (A1,A4 to A6). H15 OK (except A1) when the bias parameters are modified.

VII. LADDER 07 (LAD14)

Everything OK.

VIII. LADDER 08 (LAD04)

C1, C2, C4 and C8 bypassed. H15 with some missing chips. H15 ok when the bias parameters are modified.

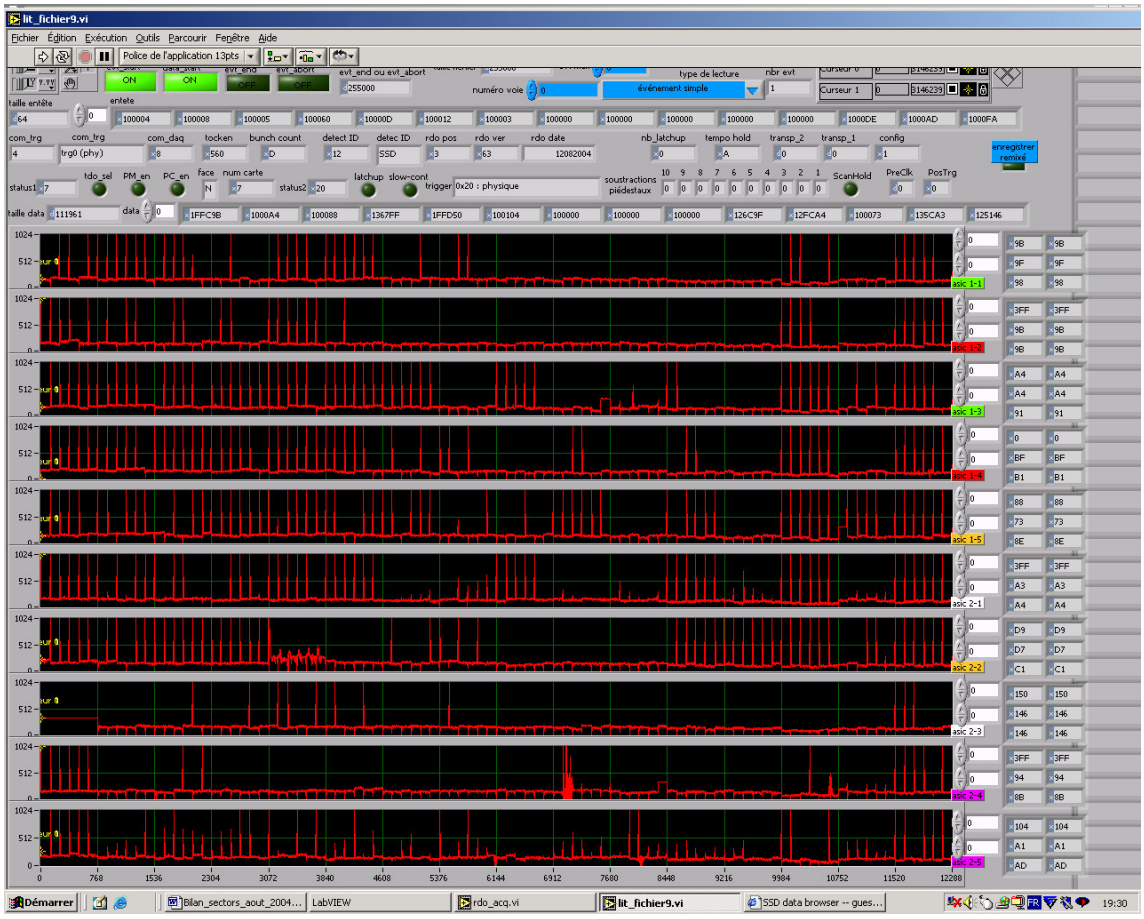
H10 with 4 a128 missing. 5 a128 are seen when A3 is bypassed.

IX. LADDER 09 (LAD05)

Everything OK.

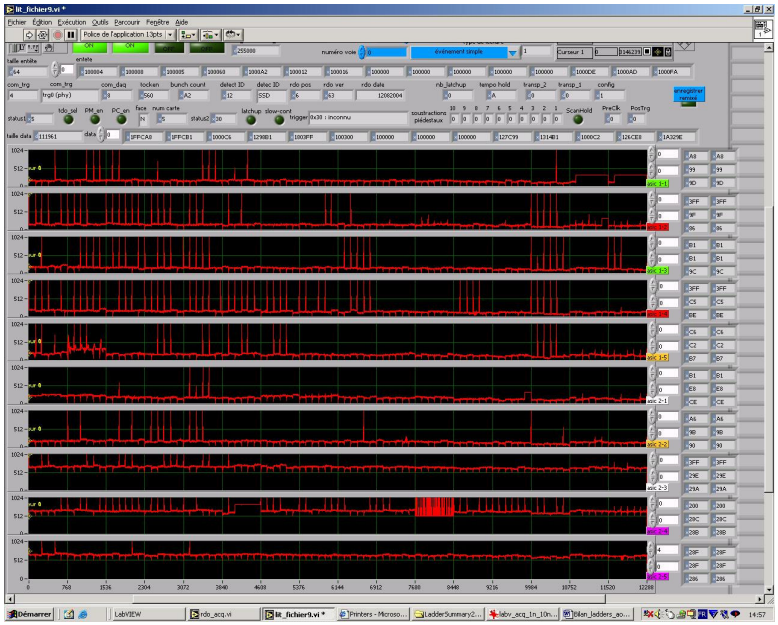
X. LADDER 10 (LAD10)

Everything OK.



Sector 1N-10N after fixing some of the problems.

Secteur 2N (11N à 20N)



All the ladders are present. The three last ladders (18,19,20) ie the ones at the end of the SCSI cable do not get their pedestals in the right range but at a value equal to the pedestal+512. We understood that this was due to a bit missing in the data from those ladders. It seems to be temperature dependant. When cold (and cool down) their pedestals are at the right place. If the pedestals jump again, we can use the offset subtraction in the read out boards.

XI. LADDER 11 (LAD15)

H15 and H16 show only the two first chips. Bias parameters changed for all the chips on these hybrids (Ipreamp=80 instead of 100 and Ishap=50 instead of 60)

No problem with H6.

C9 bypassed

XII. LADDER 12 (LAD25)

No big problem. The chip A6 on H15 is not seen. It is back when the bias parameters changed for all the chips (Ipreamp=80 instead of 100 and Ishap=50 instead of 60)

XIII. LADDER 13 (LAD16)

No problem. The chip A6 on H1 has a pedestal around 220. It should be OK.

C7 bypassed

XIV. LADDER 14 (LAD02)

No problem. C7, C8, C9 and C12 bypassed.

XV. LADDER 15 (LAD11)

H2 has some problems : bad pedestal and bigger than 255. We disconnect and plug back the bus in the Hirose connector : no change…

XVI. LADDER 16 (LAD01)

C1, C5, C12, C10, C13 and C15 bypassed

H1 ok with force bias

H6 has only 5 a128 chips !

H10 is absent frequently. OK with force bias

XVII. LADDER 17 (LAD20)

No problem. C12 bypassed.

XVIII. LADDER 18 (LAD22)

C8, C9, C14 and C16 bypassed.

The pedestal of the full ladder has some time an offset of 512 adc counts.

H11 is some time not responding (pedestal=512+/- 1). It is always ok when it is the only ladder on the SCSI cable. It is bad when the ladder 19 is on the same SCSI cable.

XIX. LADDER 19 (LAD13)

The pedestal of the full ladder has some time an offset of 512 adc counts.

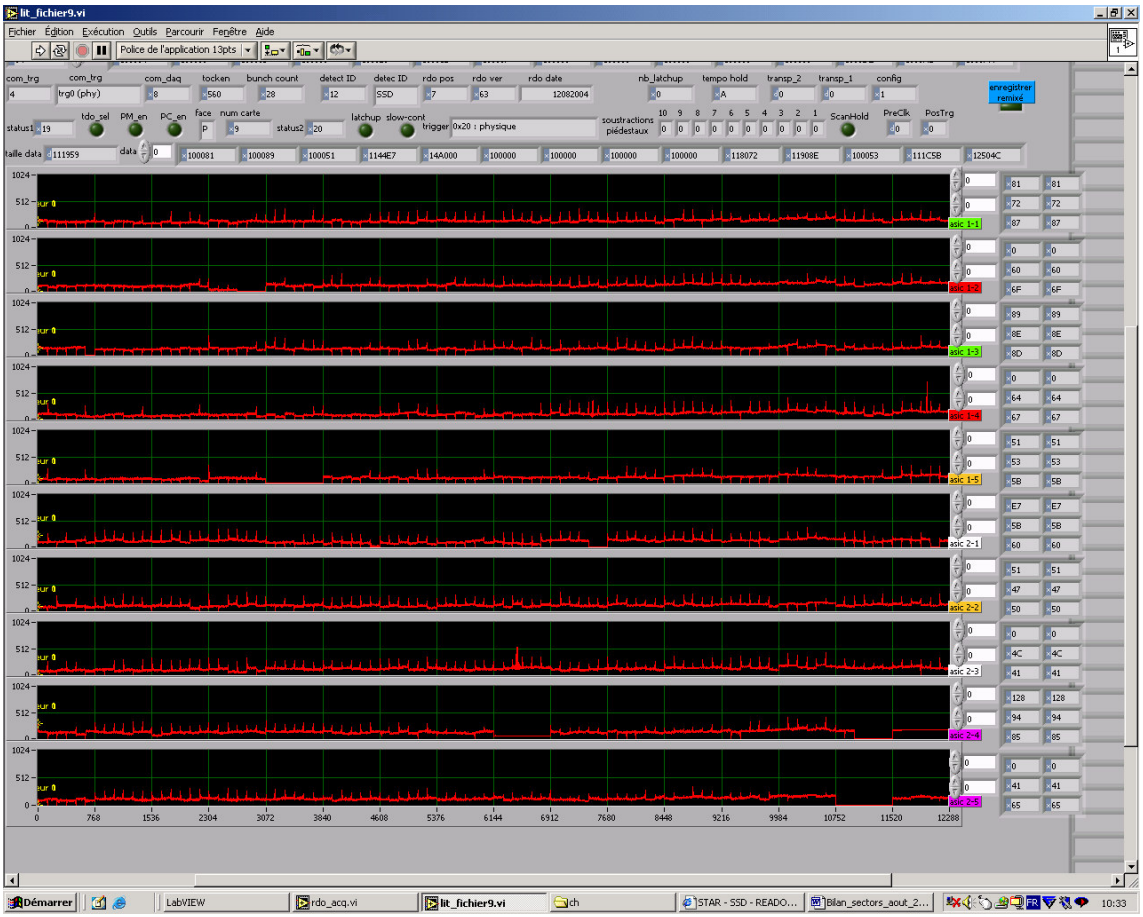
The A3 of H6 does not give any signal. When cold the hybrid gives 5 chips. When hotter, the hybrid gives less chips (A3 been always absent).

The H11 is consuming lots of current (it triggers the latchup detection) and does not give any good pedestals. Putting the chips bias to zero sets the bias at zero for the previous hybrid (H12). When alone on the SCSI cable, the H11 has is pedestal at 512.

XX. LADDER 20 (LAD08)

The pedestal of the full ladder has some time an offset of 512 adc counts.

Sector 2P (Ladders 11P to 20P)



XXI. LADDER 11 (LAD15)

Everything OK

XXII. LADDER 12 (LAD25)

Everything OK except H4 (A4 to A6 absent). A4 bypassed on H4. All the chips back except A4.

XXIII. LADDER 13 (LAD16)

Everything OK except A6 absent on H1

XXIV. LADDER 14 (LAD02)

Everything ok.

XXV. LADDER 15 (LAD11)

Everything ok except H5 absent. H5 back when A5 bypassed.

XXVI. LADDER 16 (LAD01)

Everything OK when H4, 5 and H13 are with force bias.

A5 and A6 absent on H10. A6 is back when A5 is bypassed.

A5 absent on H16

XXVII. LADDER 17 (LAD20)

Everything ok.

XXVIII. LADDER 18 (LAD22)

Everything OK. Noisy area in H9.

XXIX. LADDER 19 (LAD13)

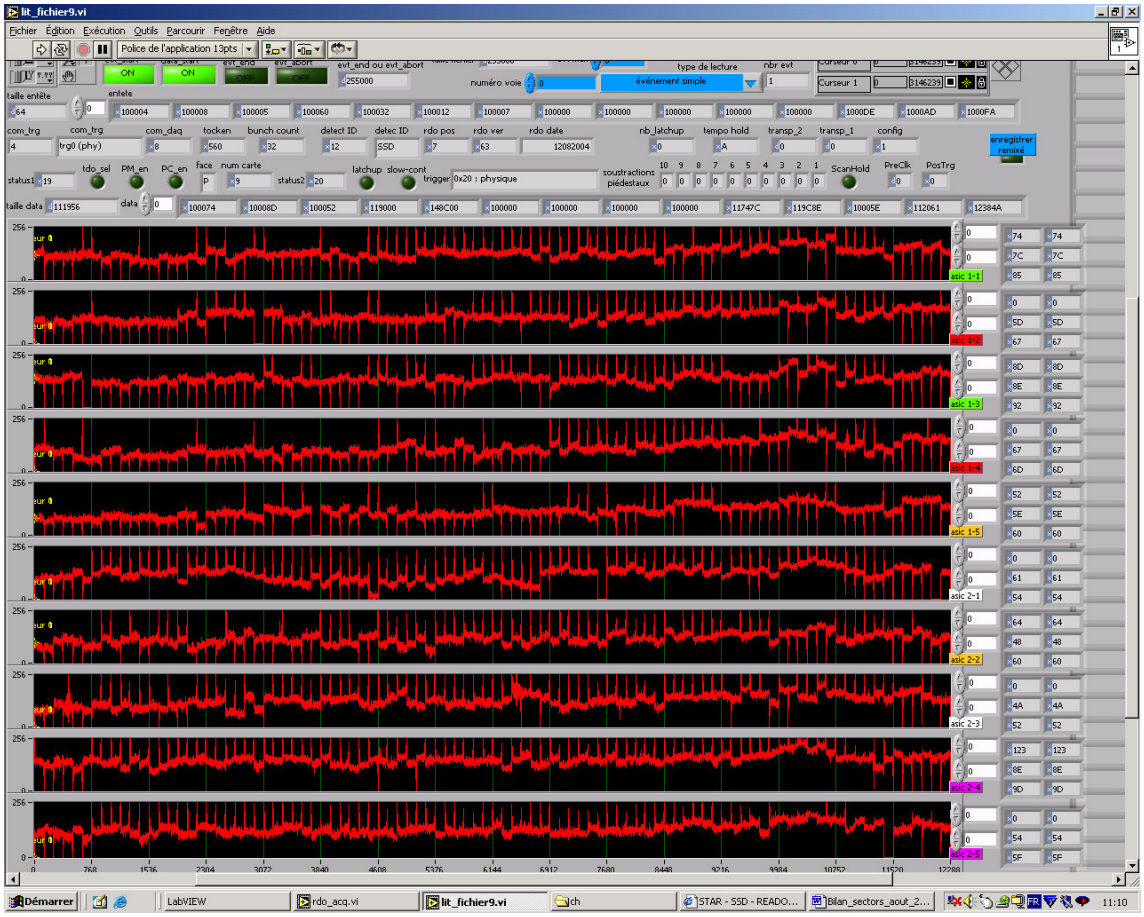
H3 always present !!!

H9 absent, H16 absent, A3 to A6 absent on H15

H15 and H16 OK with force bias. H9 back without changing anything

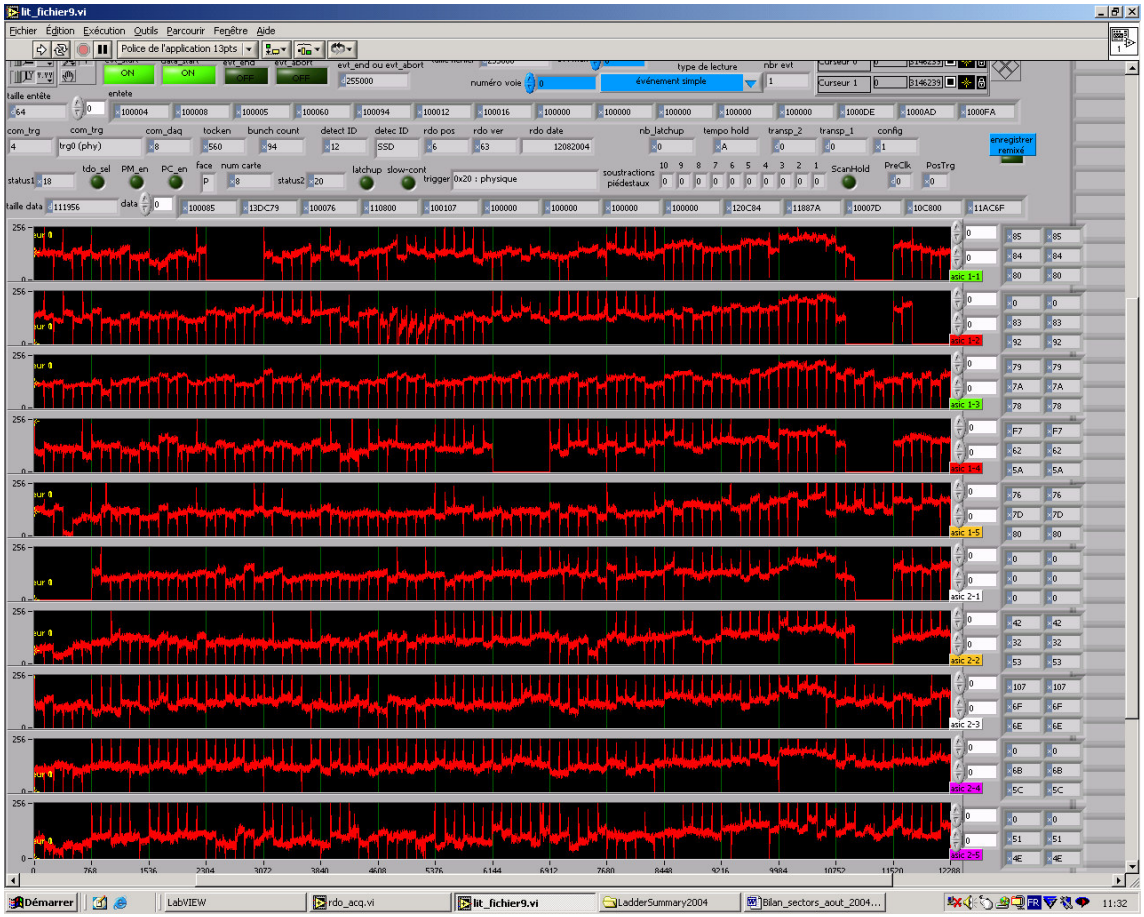
LADDER 20 (LAD08)

H15 absent. OK when A2 is bypassed



Sector 2P after the changes.

Sector 1P (ladders 1P to 10P)



1. Ladder 1

Everything OK

2. Ladder 2

Everything OK

3. Ladder 3

Everything OK

4. Ladder 4

A3 to A6 missing on H15. OK with bias parameters changed

5. Ladder 5

H1 missing. Still missing with force bias.

A3 to A6 missing on H15. OK with bias parameters changed

6. Ladder 6

Everything ok

7. Ladder 7

A2 to A6 missing on H15. OK with bias parameters changed

H9 missing. All chips back when A1 is bypassed.

8. Ladder 8

Everything is ok. Seems to dislike the heat.

9. Ladder 9

A2 to A6 missing on H15. OK with bias parameters changed

A3 to A6 missing on H16. OK with bias parameters changed

The pedestal on H7 has a bad shape.

10. Ladder 10

A3 to A6 missing on H15. OK with bias parameters changed except A1 with high ped. A1 is sometimes ok when it has its bias set to the nominal value

H4 missing. Back with force bias.