Part III

Essential Model with Words

Chapter 18

Electronics/Interfaces/DAQ

Last Updated: 15 June 1995

18.1 SVT Electronics Context

The SVT consists of 216 Silicon Drift Detectors (SDD) located on 3 concentric barrels. It is positioned near the center of the STAR detector.

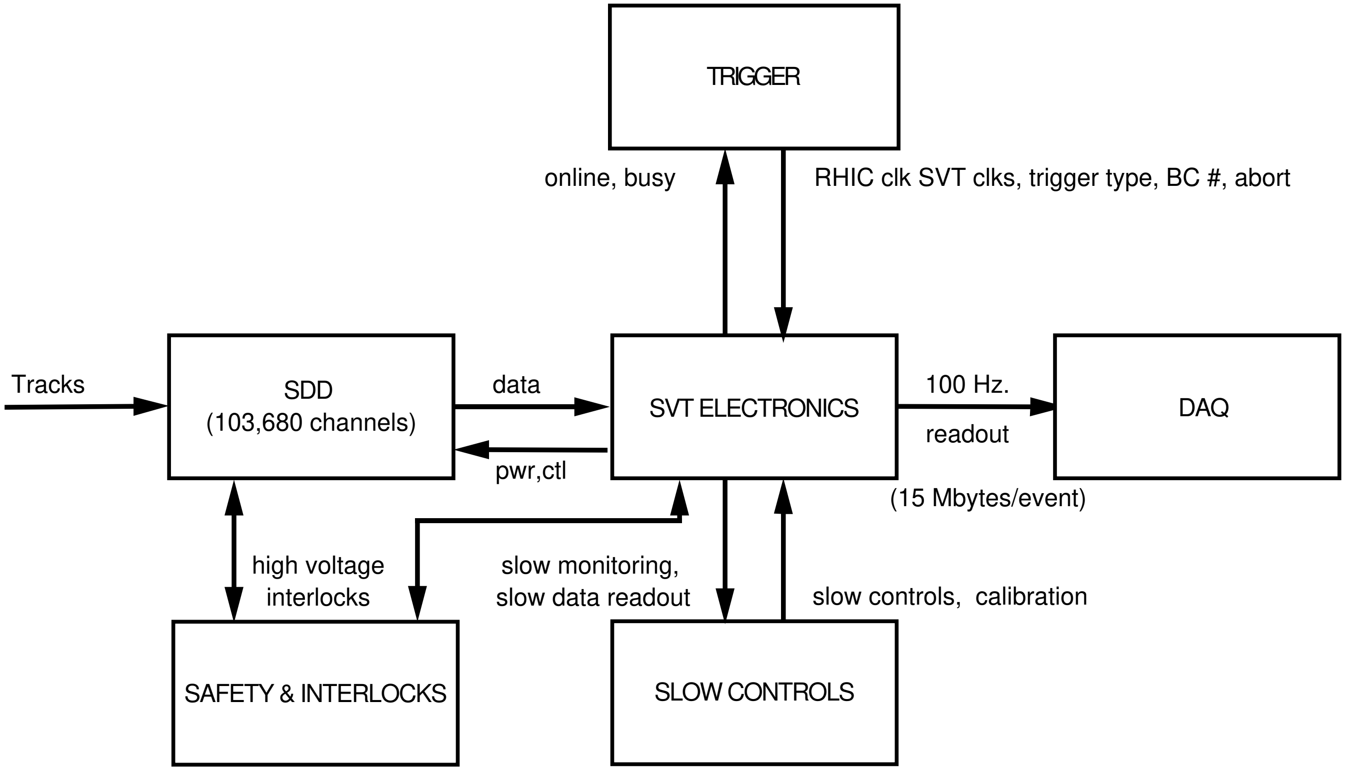
The SDD is a bidirectional drift detector with 240 anodes on opposite sides (480 anodes total, each SDD). Therefore the SVT has 103,680 anode channels total.

Each central collision of relativistic heavy ions may result in thousands of energetic charged particles whose trajectories pass through the SDDs. Most trajectories (tracks) will pass through the silicon with little nuclear interaction or deflection. However, as they pass through the detectors the silicon is ionized along the path of each track. Shaped electric fields exist in the SDDs, and the ionization electrons drift to the edges (anodes) of the SDDs. Usually each track leads to signals on 2 – 5 anodes, depending upon details. The signals have a time width on the order of 100 ns.

Electronics next to the SDDs amplify and time-sample the anode signals (128 time samples per anode). The analog data are passed to the SVT Electronics (a short distance away from the SVT) for analog-to-digital conversion and transfer (via fiber optics) to the Data Acquisition System (DAQ) located in the STAR counting house.

The Electronics are interfaced to DAQ via 24 fiber optics cables, each capable of transmitting data at more than 1 Gb/sec. The system is capable of data throughput to DAQ of 100 events/sec.

Timing for the SVT electronics is generated by the Trigger System which interfaces to the Electronics. Control and Monitoring is via Slow Controls. Interlocks are required for a variety of protection and safety issues.



SVT ELECTRONICS CONTEXT

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18.2 SVT Electronics – 0.0 and SVT Electronics – 0.1

The SDDs and associated preamps, storage devices and interfaces are on the Detector Ladders that make up the barrels of the SVT. The hybrids contain (1) PASAs (Preamplifier and Shaping Amplifier), (2) SCAs (Switch Capacitor Array), and (3) Multiplexing Electronics. The SCAs time sample the signals from the PASAs. The Multiplexing Electronics reduce the number of cables needed to remove data from the Ladders.

The Sector Electronics (1) contain clock drivers to provide the Timing for readout of the SCAs on the Ladders, (2) provide Analog to Digital conversion of the data from the Ladders, (3) provide multiplexing for the Analog to Digital conversion, (4) prepare the data for transmission to DAQ, and (5) transmit the data to DAQ. They also (6) provide power for the Ladder electronics. Timing and control is received from the Trigger/Clock distribution is used locally, and is passed on to the Ladder electronics. The Clock generator includes a section specific to the SVT.

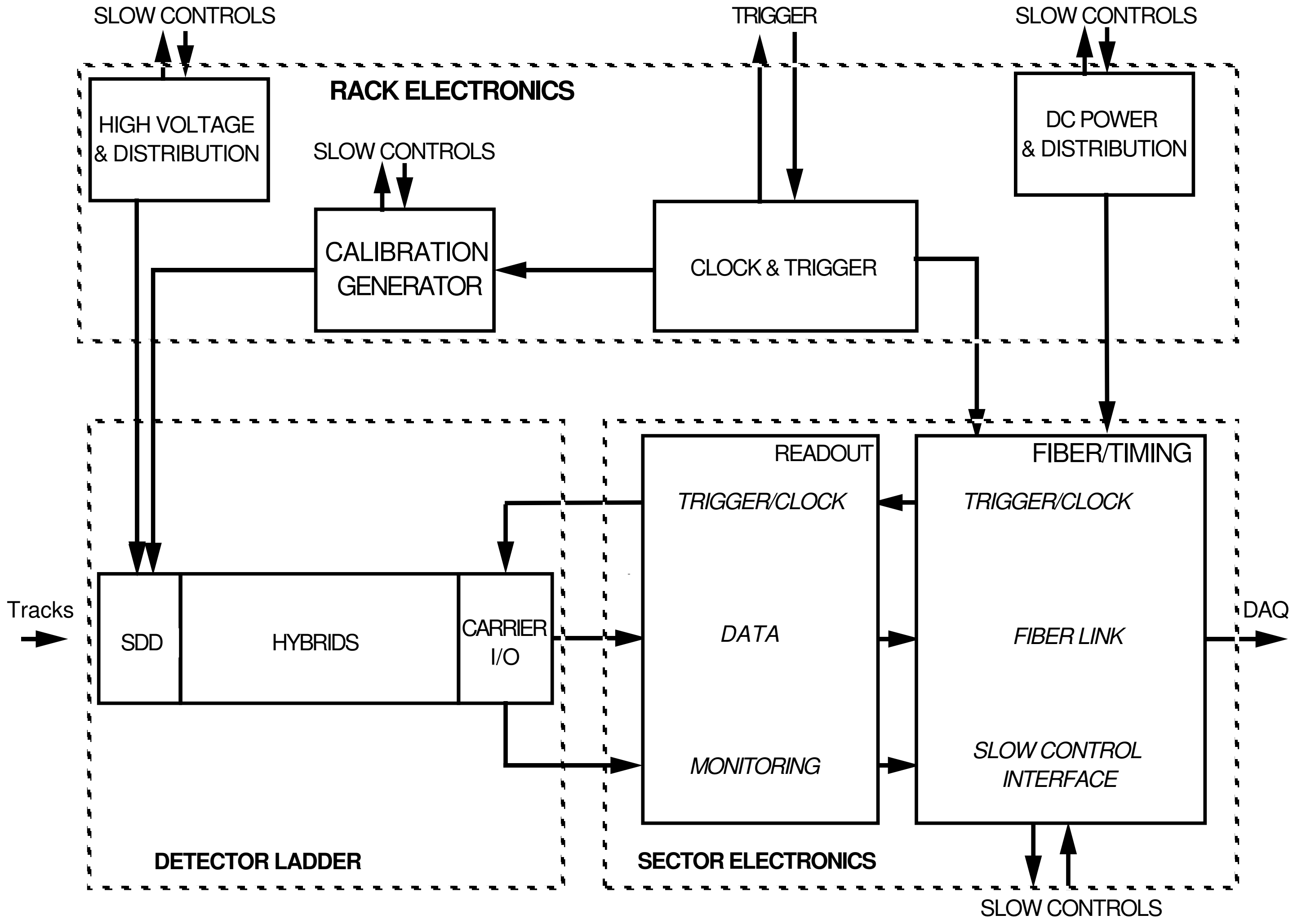
The Rack Electronics consist of (1) High Voltage Power Supplies, (2) Low Voltage Power Supplies, (3) a Calibration Generator, and (4) SVT Clock/Trigger Distribution. The High Voltage power is for the SDDs. The Low Voltage Power is for the Ladder and Readout Electronics. The Calibration Generator allows calibration of the SDDs through charge-injection of known charge. The Clock/Trigger provides clocks for generating various timing signals and triggers the readout of data.

The electronics on the Ladders interface to (1) the Sector Electronics at the STAR TPC Wheel (through the Carrier I/O), (2) the Calibration Generator in the racks, and (3) High/Focusing Voltage in the racks, via multiple cables.

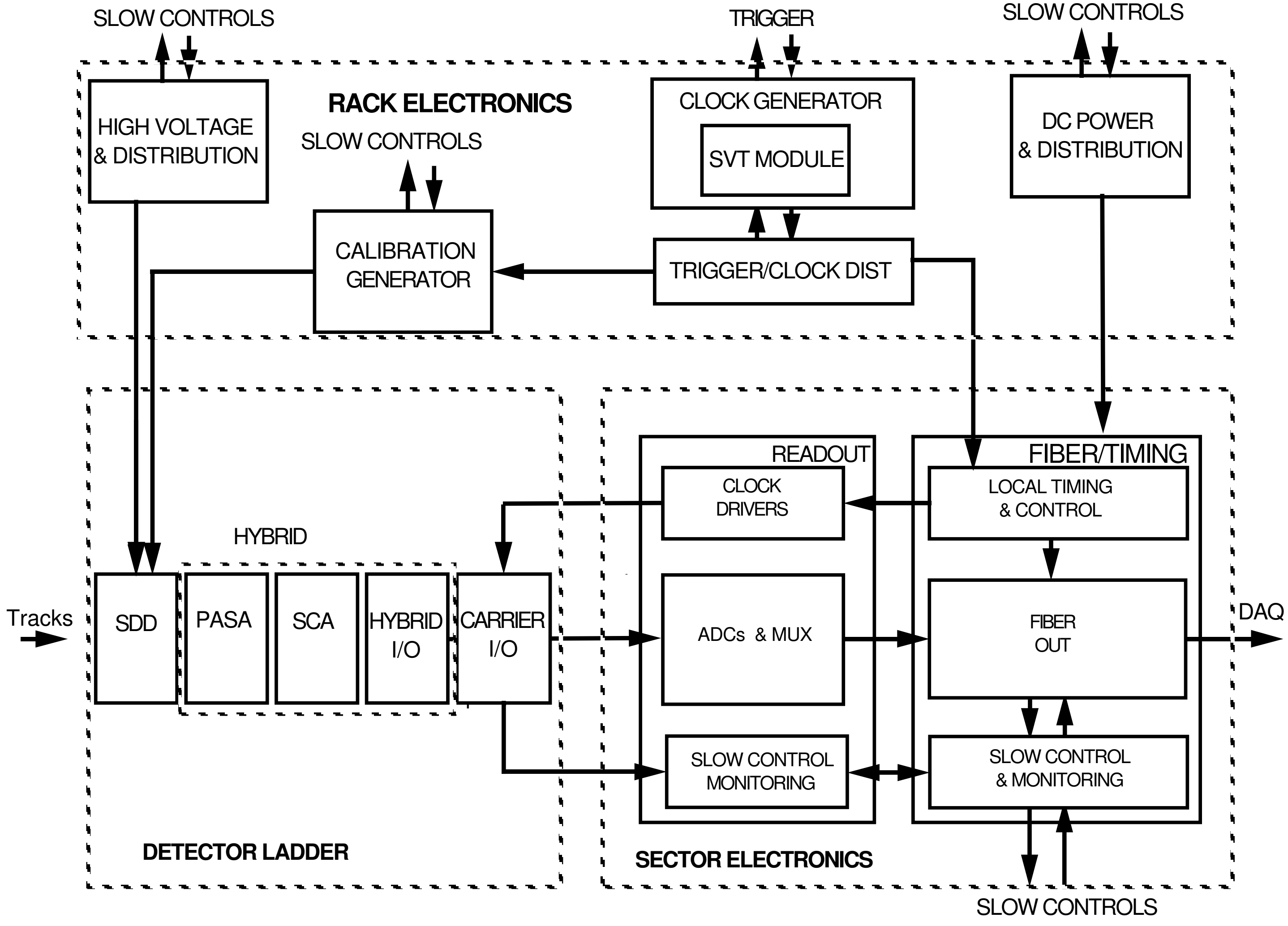
The Sector Electronics interface to (1) the Ladder electronics, (2) the Clock/Trigger Distribution, (3) Slow Controls, (4) DC power, and (5) DAQ, via multiple cables.

Controls also interfaces to (1) High Voltage, (2) DC Power, and (3) the Calibration Generator.

The SVT Clock/Trigger interfaces to STAR Clock/Trigger.



0.0 SVT ELECTRONICS rhm 1/11/95



0.1 SVT ELECTRONICS

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18.2.1 Carrier Electronics

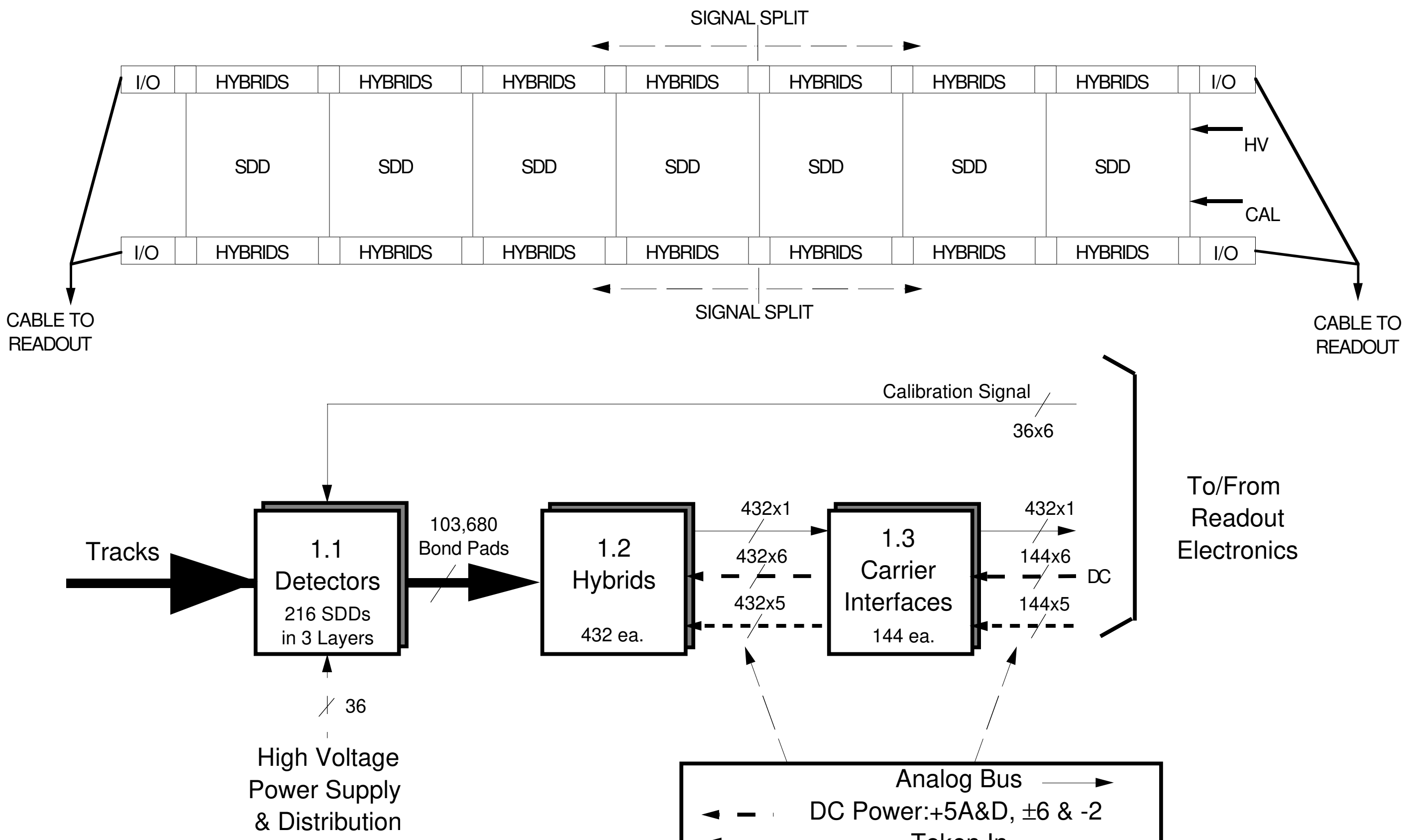
The SVT contains 36 Ladders which are arranged to form 3 concentric barrels. Each Ladder contains one detector carrier and two electronics carriers. A total of 216 SDDs are mounted on the Ladders. Since each SDD has 480 anodes, there are 103,680 total anodes.

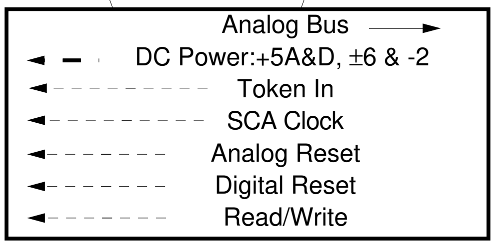
Each (detector) carrier has either 4, 6 or 7 SDD wafers, depending on its location in the SVT. Hybrids immediately adjacent to the SDDs contain the PASAs and SCAs for readout of the pulses from the SDDs. The SDDs are bidirectional. One half of each SDD drifts down (using convention shown in the figure), and the other half drifts up. Each hybrid services 1/2 of an SDD (or 240 anodes), so there are a total of 432 hybrids. For each hybrid the SCA output is multiplexed to an Analog Bus. Since each Analog Bus contains information from 240 anodes, the multiplexing is 240:1.

Two Carrier Interfaces are located on each end of each Ladder (one on each end of each Hybrid Carrier). There are a total of 144 Carrier Interfaces. These are the (I/O) interfaces to the Readout Electronics. Carriers are readout from each end. For the 7 SDD Ladders, 3 SDDs are read out one end, and 4 SDDs are read out the other end.

DC Power and SCA timing/control signals are delivered to the Hybrids via the Carrier Interfaces.

Calibration signals are fed to the SDDs to inject a test signal for gain and offset calibration.





LAYER	SDDs	STICKS X	HYBRIDS/STICK=	HYBRIDS
OUTER	112	32	7	224
MIDDLE	72	24	6	144
INNER	32	16	4	64
	216	72		432

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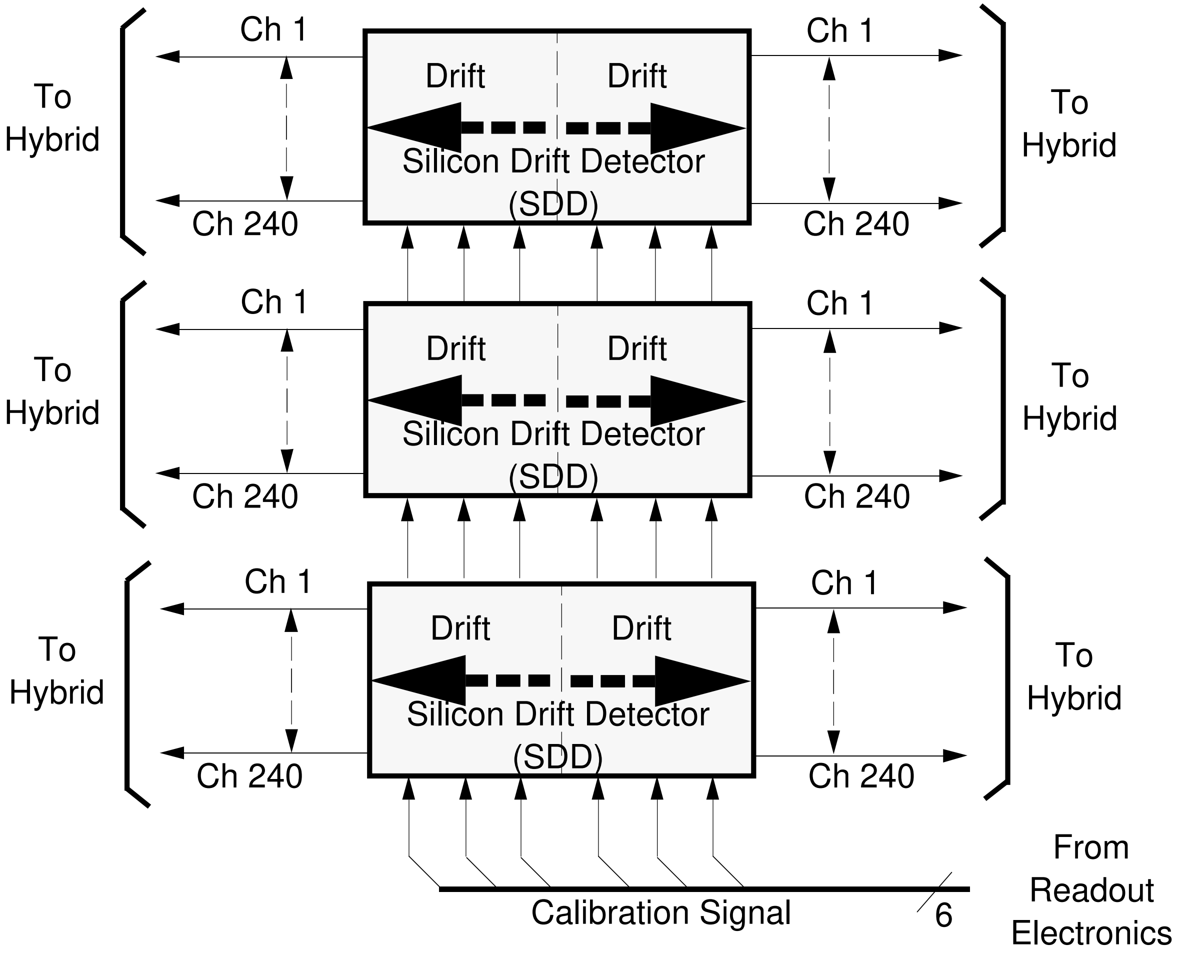
1.0 Carrier Electronics

18.2.1.1 Detector – 1.1

Silicon Drift Detectors (SDD) are novel position sensing silicon detectors which operate in a manner analogous to gas drift detectors.

A 4 inch, high resistivity (around 3 KΩ/cm) n-type Si wafer is used as a substrate. Field shaping electrodes are constituted of p-type material implanted symmetrically on both surfaces in a regular strip pattern. The pitch between cathodes in the STAR SDD prototypes is 120 μm. A high voltage gradient (up to 600 V/cm) applied to these shaping electrodes fully depletes the Si thus creating a deep potential well that attracts free electrons produced by the passage of charged particles through the detector. The surface electrodes are symmetrically connected to a voltage divider network that produces an independent electrostatic field parallel to the surface of the wafer. The field transports the electrons towards the edge of the detector where signals are read out on a segmented anode (pitch = 250 μm). Under suitable conditions, the electron drift velocity is constant, so that a measure of the drift time is equivalent to a measurement of the position in the drift direction. During drift, with typical speed of 1 $cm/\mu s$, the initial cloud of electrons expands due to diffusion and Coulomb repulsion. The charge thus read out is shared among few anodes (2-5) over a somewhat extended time period (few 100 ns).

The ionization electrons in each SDD drift to the anodes. Drift is from the center to the edges (bidirectional drift), so there are 240 channels from each SDD to each Hybrid and 480 channels total for each SDD. Calibration and high voltage distribution is to the end of the carrier and daisy chained half the length of the carrier. Since the drift velocity is temperature sensitive, the SDD is air cooled using a closed system air conditioning system. The electronics carriers are water cooled.



1.1 Detector

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18.3 Hybrid – 1.2

Each Hybrid services one half of an SDD (240 anodes). 432 Hybrids are required for the SVT. Each Hybrid contains 15 PASAs and 15 SCAs plus their support electronics. The Hybrids use a beryllia substrate to minimize radiation length and still provide adequate strength. The Hybrid carrier is water cooled to provide the temperature stability needed to insure consistent drift behavior in the SDD.

18.3.0.2 PASA – 1.2.1

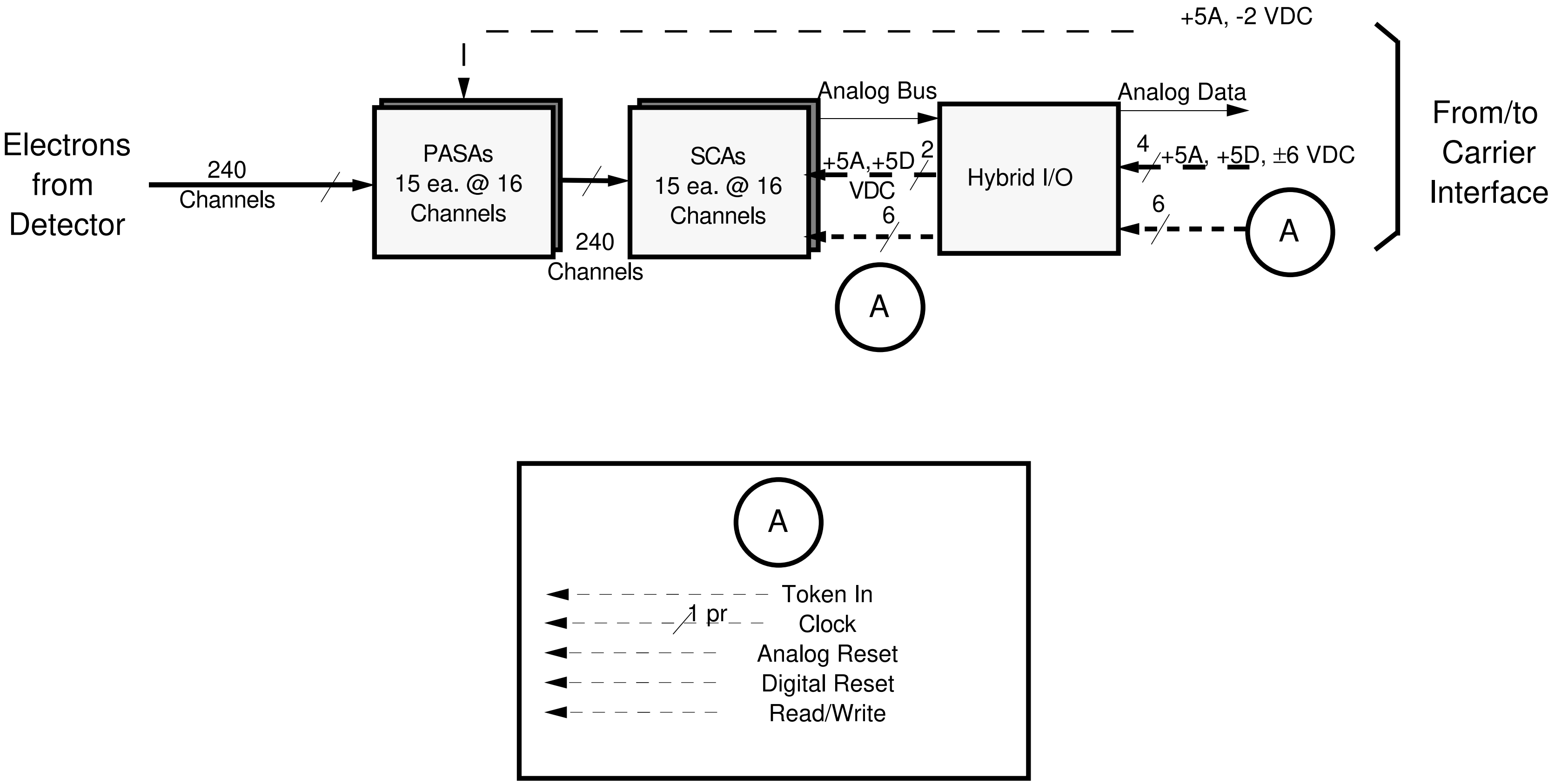
Each PASA has 16 channels. 15 PASAs are included in each Hybrid to cover 240 channels. Connection from the SDD to the PASA is via wire bonds.

18.3.0.3 SCA – 1.2.2 and SCA Organization – 1.2.2.1

The SCA has 16 channels providing analog storage in a circular buffer. Data is stored and overwritten until a trigger stops storage and readout begins. 15 SCAs are combined on one Hybrid to cover 240 channels. Readout is started by passing a Token to the first SCA causing the first time sample of the first channel to be read out first, followed by subsequent channels until all 16 have been read out. The token is then passed to the next SCA and so on until all 240 channels have been read out. A new token is then sent to the first SCA which causes the readout of the first channel's second time sample, and the process continues for all channels. 128 tokens are passed to the SCAs to read out all 128 time samples. Each SCA provides analog output for all 16 channels; the 15 SCA outputs are multiplexed onto 1 analog bus, resulting in a 240:1 multiplexing ratio.

18.3.0.4 Hybrid I/O – 1.2.3

Each Hybrid includes an I/O and control section to support the PASA and SCA. The Hybrid I/O receives and distributes the SCA clocks and control signals as well as the DC power for the SCA and the PASA. The output from the SCAs is buffered.



1.2 Hybrid
(1 of 432)

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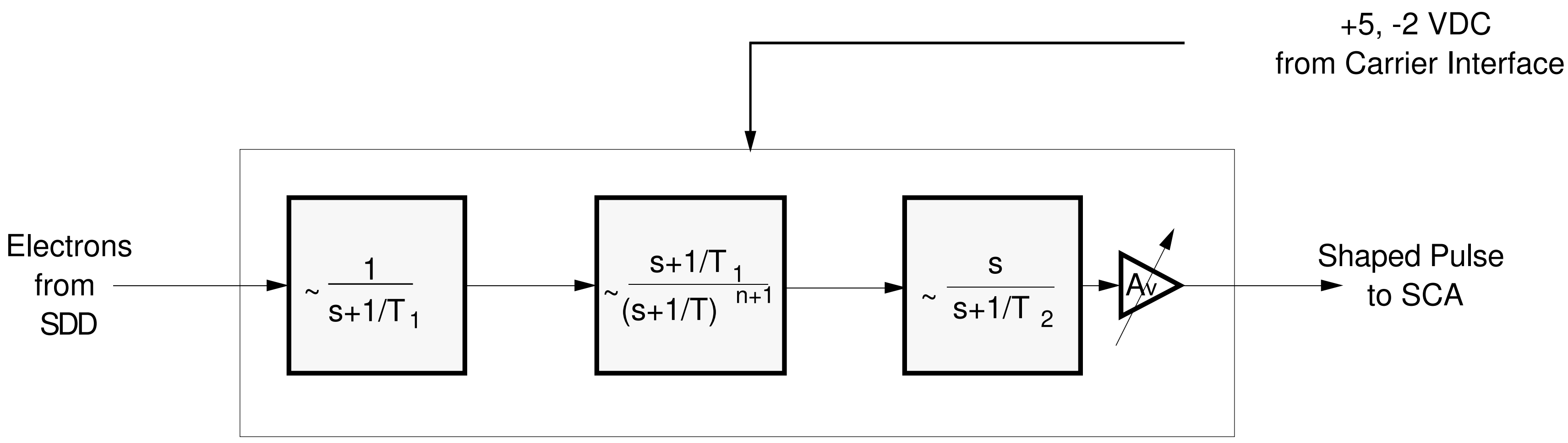

Notes:

Channels depicted 1
Channels per Shaper 16
Shapers per Hybrid 15
Channels per hybrid 240

Electrical Characteristics:

Peaking time ~50 ns
Power dissipation < 5mW/channel

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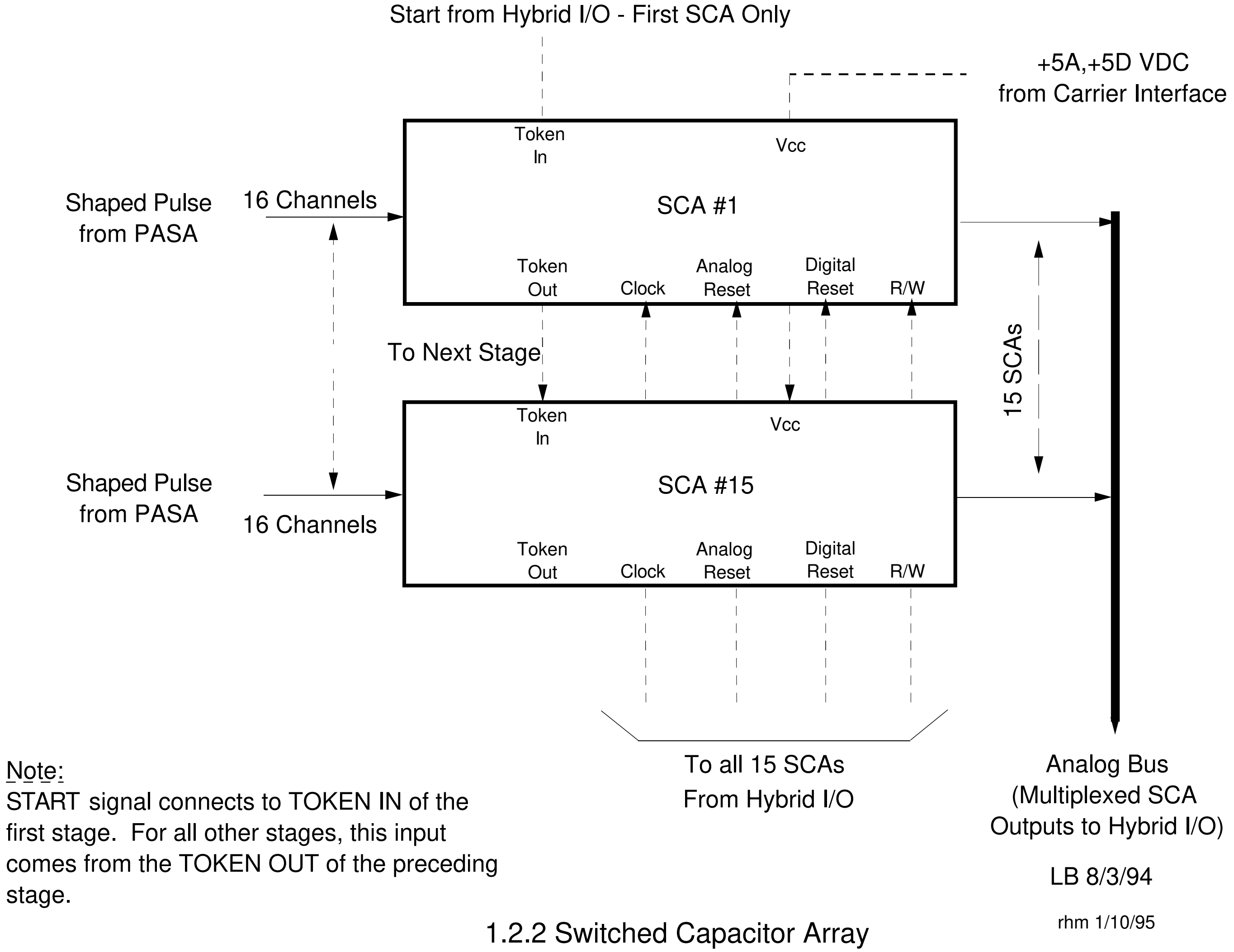
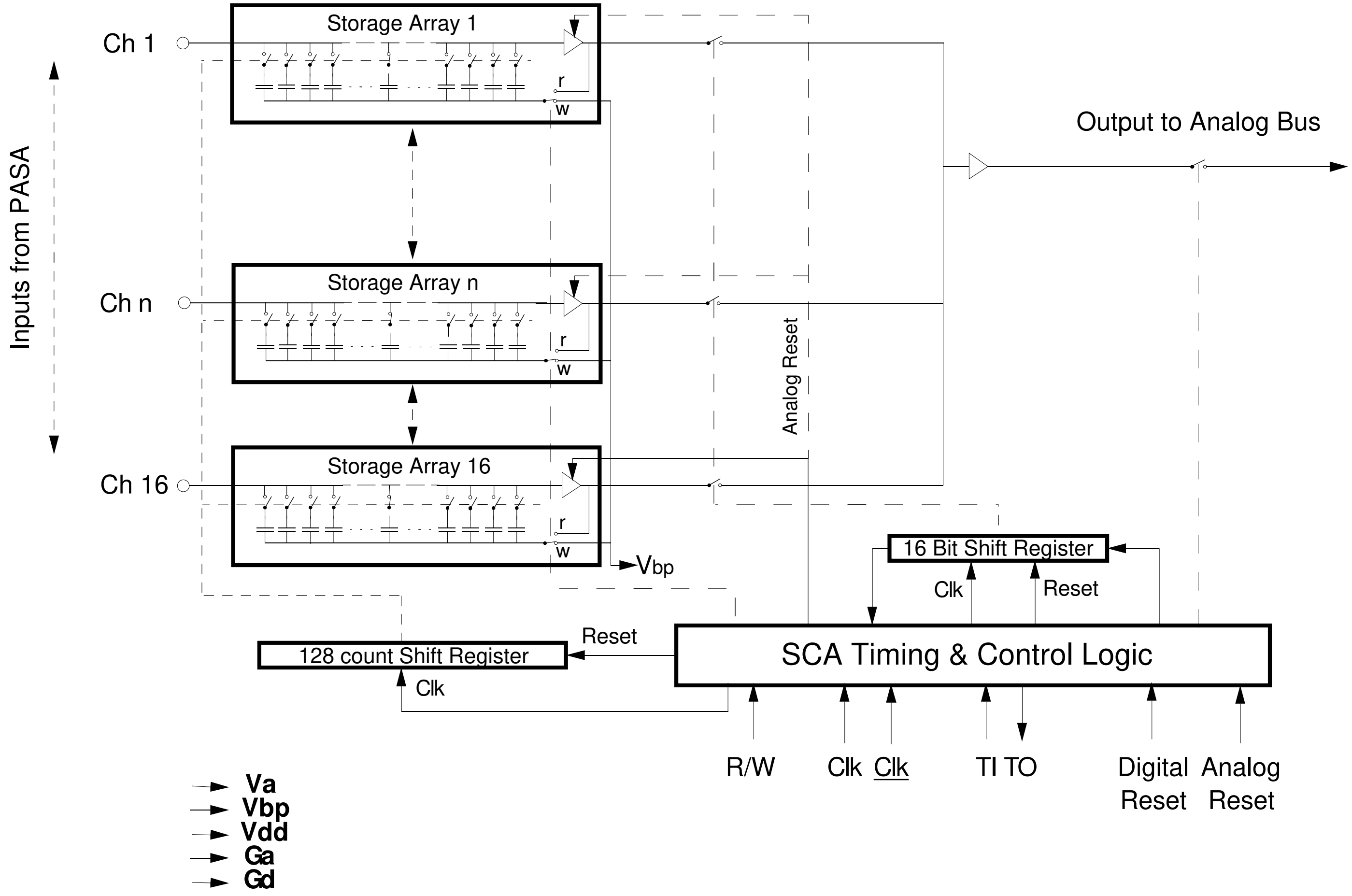
1.2.1 PASA

(1 of 16 Channels/Shaper)



1.2.2 Switched Capacitor Array
(showing on-hybrid interconnects)



1.2.2.1 SCA Organization
(Switches shown in write state)

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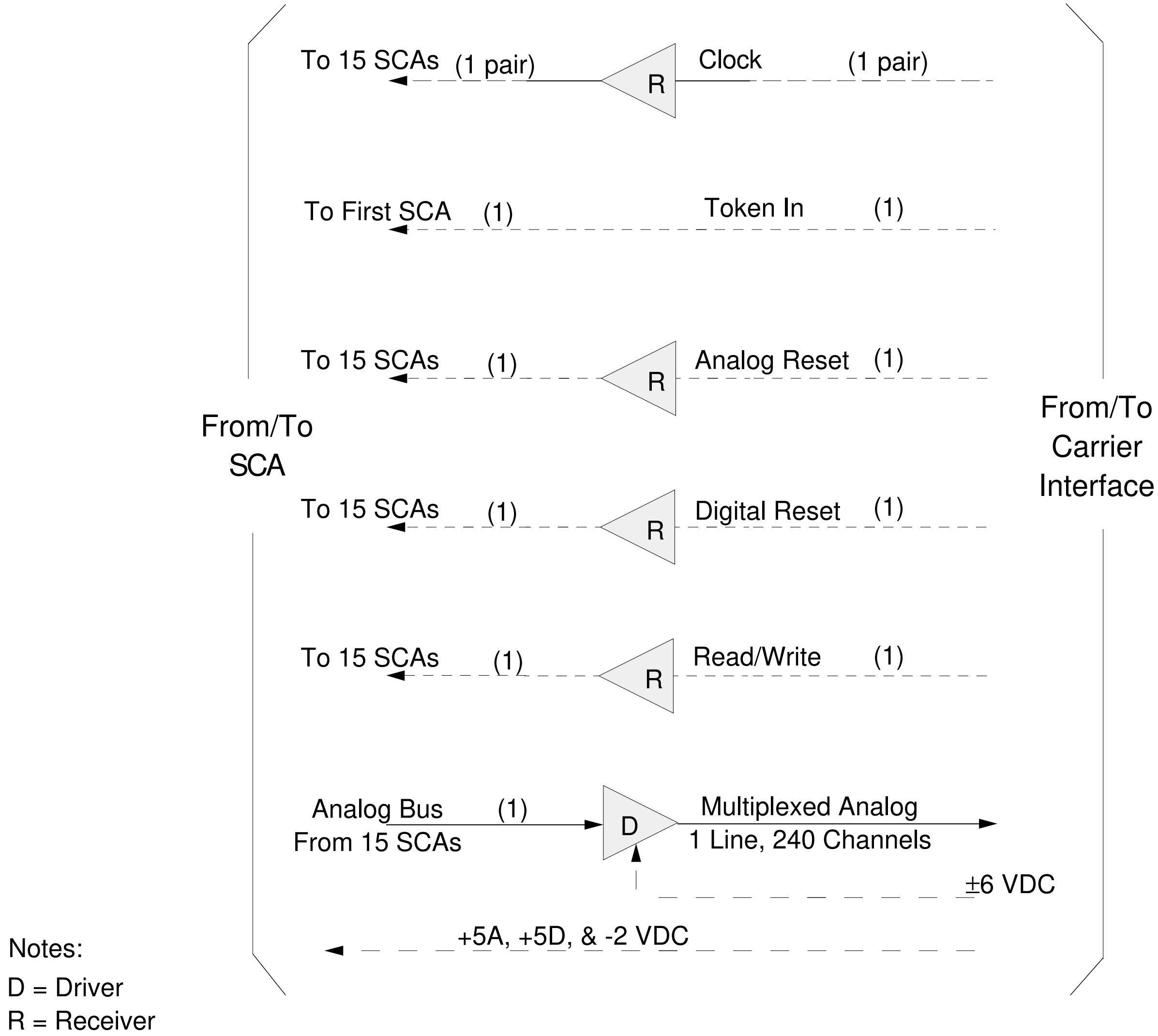

1.2.3 Hybrid I/O
(One Hybrid)

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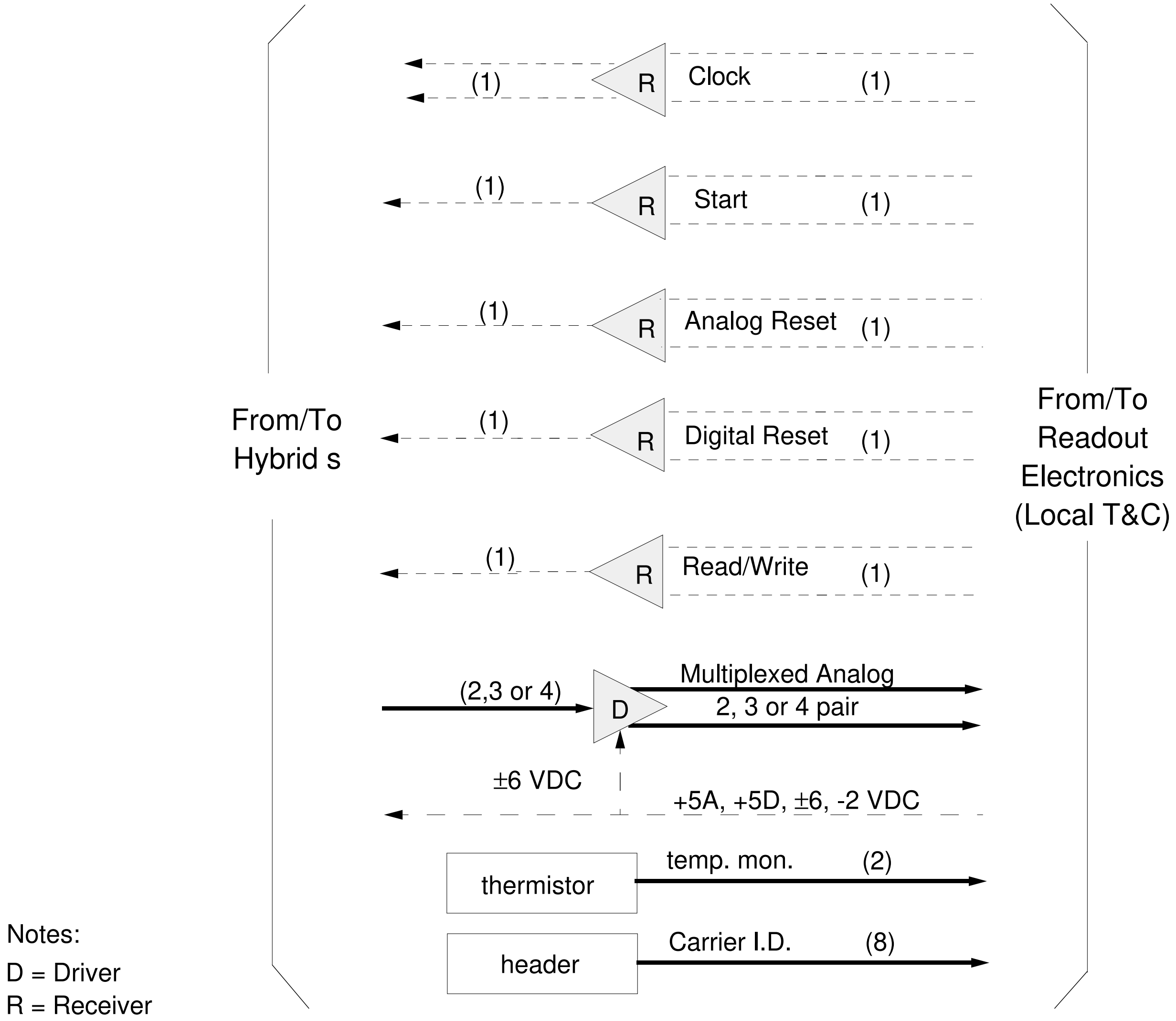
18.3.1 Carrier Interface – 1.3

There are 4 Carrier Interfaces per Ladder (one on each end of each Hybrid carrier); the total number of Carrier Interfaces is 144. The Carrier Interfaces buffer and distribute SCA control signals, DC power and analog outputs. In addition, temperature monitoring is routed through the Carrier Interface and a unique serial number ID is provided each Carrier Interface to validate cabling when in operation.



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1.3 Carrier Interface
(Each end of each Carrier Side, 1 of 144)

18.3.2 Readout Electronics – 2.0

There are 24 Readout Electronics sectors to service the 216 SDDs of the SVT. Each Readout Electronics sector is divided into a receiving section and a transmitting section. Input to an individual readout sector includes 9 detectors and in some cases is split between SVT layers.

The Receiving section (1) sends timing and control information to the Hybrids for readout of the analog data, (2) contains Analog to Digital converters for the Multiplexed Analog data received from the Carrier Interfaces, (3) multiplexes the digital data for the Transmitter, (4) receives monitor data from the Carriers and prepares it for Slow Controls readout, and (5) provides DC power to the Carrier Interfaces.

The Transmitting section transfers data to DAQ via fiber links at 1.2 Gbps.

The Readout Electronics interface to DAQ, SVT Clock/Trigger Distribution, and Slow Controls.

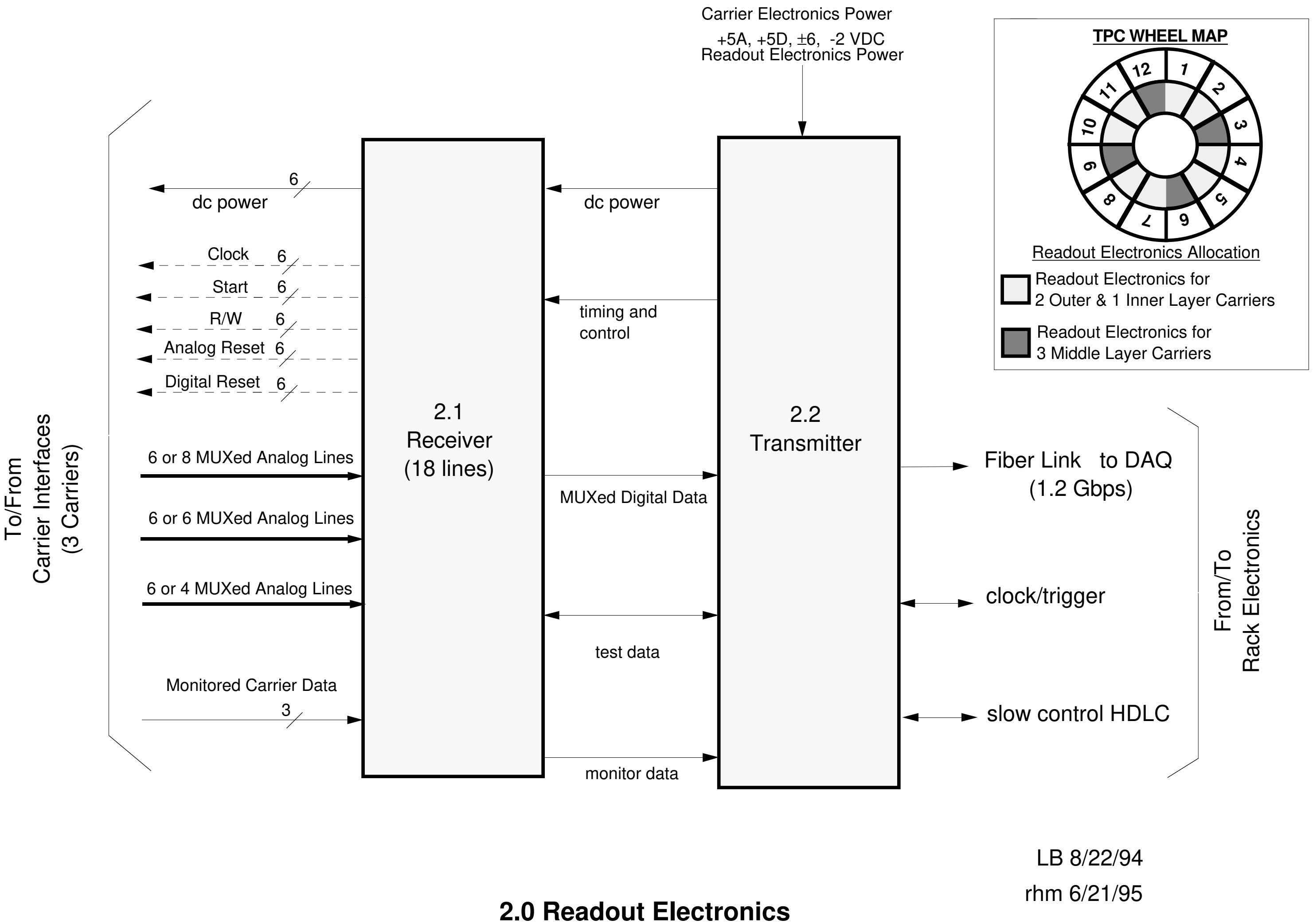
The Readout Electronics receives ± 8 VDC power from power supplies in the SVT racks, and power conditioners located in the Readout Electronics sectors generate the voltages required by both the Readout Electronics and the Carrier Interfaces.

18.3.2.1 Receiver – 2.1

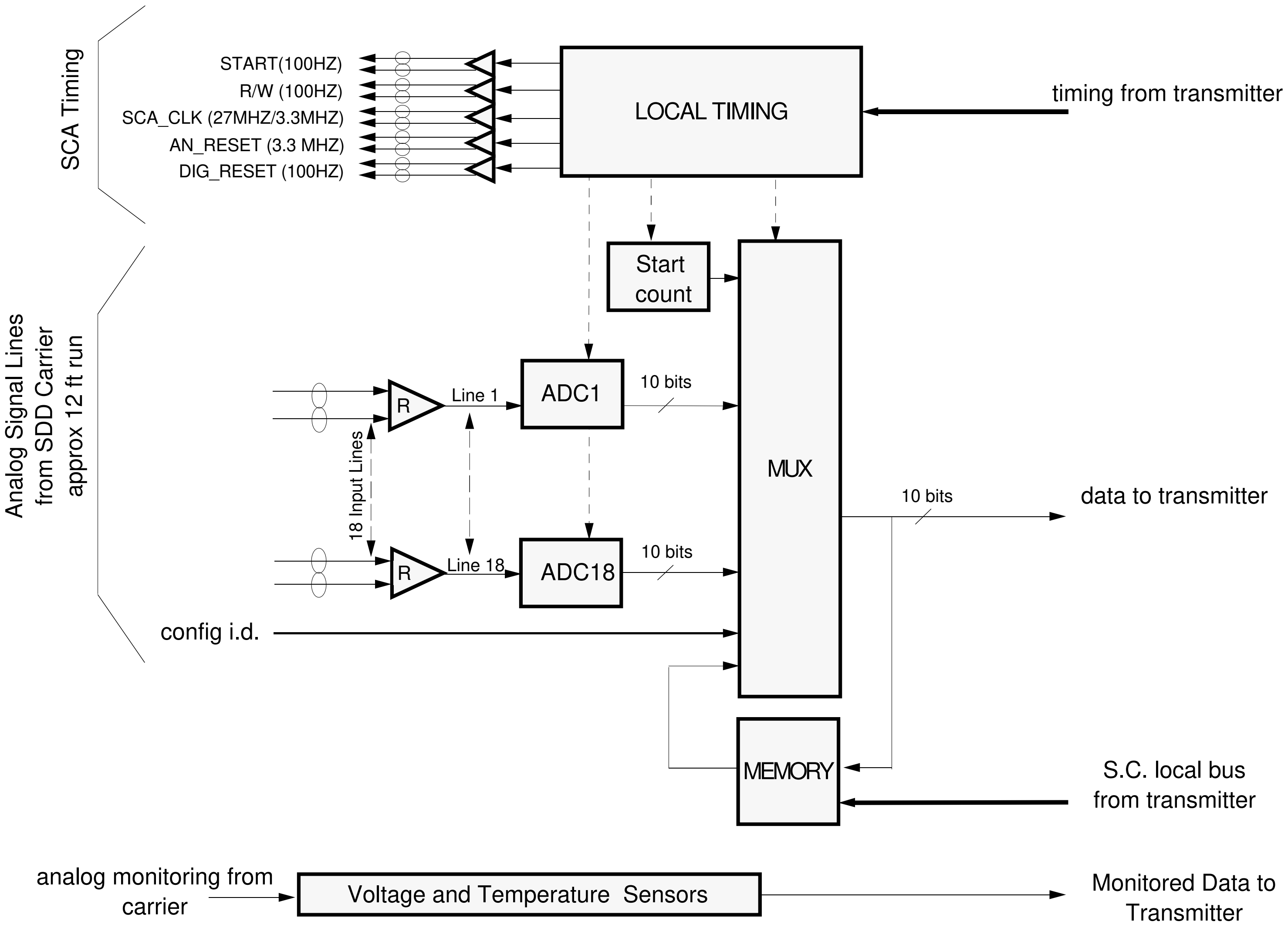
The 18 analog inputs are digitized by 18 10 bit analog to digital converters. Digitization can be delayed for 100 μs to avoid interference from/to the STAR TPC. Local timing is derived from the clock and timing inputs, and SCA timing control is passed to the detectors. Local memory is provided to capture data locally for debugging purposes, and test data may be loaded or read to or from it via the Slow Controls interface. On-card voltages and temperature are monitored. Carrier monitored data are passed on to Slow Controls.

18.3.2.2 Transmitter – 2.2

10 bit data are combined with header information to supply data to the fiber link.



2.0 Readout Electronics
(1 of 24 Sector Units)



2.1 RECEIVER

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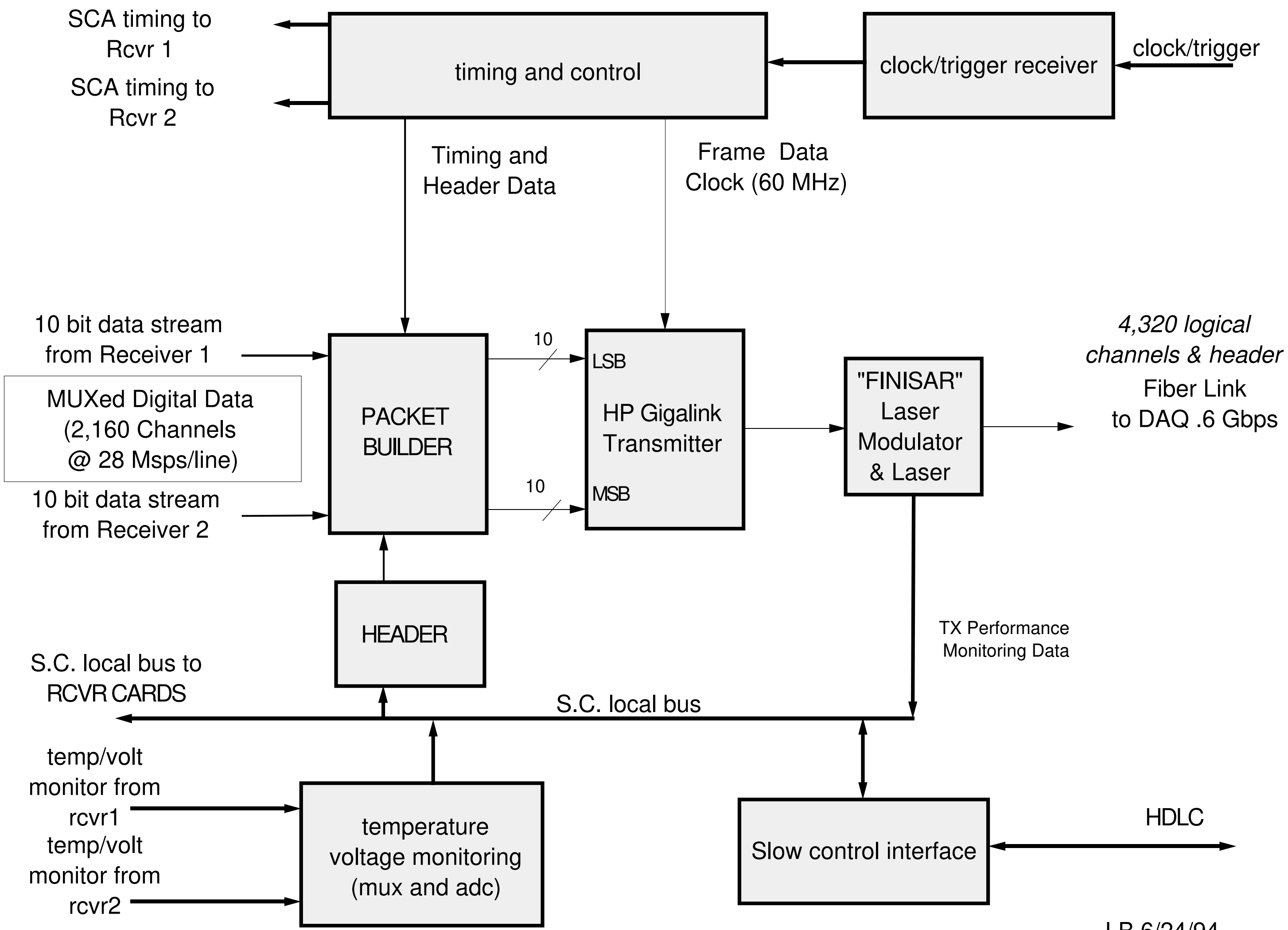

2.2 Transmitter
(1 of 24 Sector Units)

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18.3.2.3 Detector Readout Electronics Mapping for One Quadrant

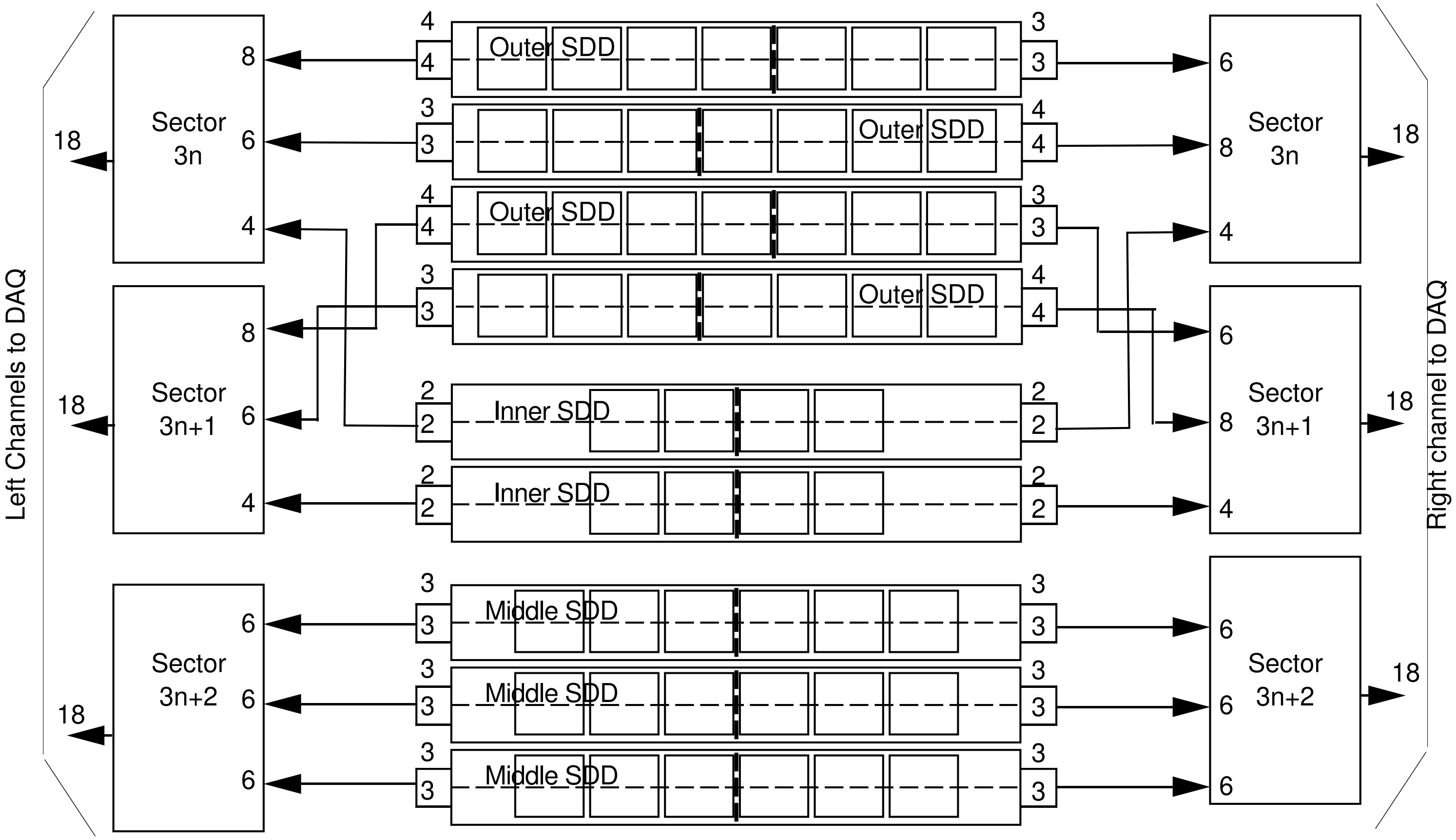
It is necessary to mix and match layers in the readout to match the granularity of the readout modules and to minimize the effect of a single module failure.

There are 12 Readout Electronics locations on each TPC endcap (total of 24 Readout Electronics locations). For the figure, there are left Sectors and right Sectors, and the value of Sector ranges from 0 to 11.

For right and left Sectors 0, 3, 6, and 9, the mapping is as follows: 4 Outer Barrel SDDs from one Ladder, 3 Outer Barrel SDDs from another Ladder, and 2 SDDs from an Inner Barrel Ladder. Two Hybrids serve each SDD, so there are 18 multiplexed analog lines to each of these Sectors.

For right and left Sectors 1, 4, 7, and 10 the mapping is the same as above.

For right and left Sectors 2, 5, 8, and 11 the mapping is as follows: 3 Middle Barrel SDDs from one Ladder, 3 Middle Barrel SDDs from another Ladder, and 3 Middle Barrel SDDs from yet another Ladder. Two Hybrids serve each SDD, so there are 18 multiplexed analog lines to each of these Sectors.



Notes:1-Numbers on lines are groups of
240 multiplexed channels
2-two hybrids serves one SDD
3-values of n are 0,1,2 and 3

DETECTOR-READOUT ELECTRONICS
MAPPING FOR ONE QUADRANT

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18.3.3 Rack Electronics – 3.0

Rack Electronics includes Timing and Control, Calibration and Slow Controls. The Timing and Control is generated in the Trigger Rack with an SVT specific Trigger/Clock distribution. The Calibration Signal Generator is configured via Slow Controls and sends pulses to the SDDs for calibration. Slow Controls interfaces are of two types: one to/from the Sector Electronics and one for everything else.

18.3.3.1 Master Timing and Control – 3.1

The SVT specific timing card is based on the trigger circuitry common to all systems but includes the SVT specific control. Trigger CMD words, token words, etc., are sent to the Sector Electronics where local circuitry responds to STAR trigger commands. Command words are delayed appropriately. SCA clocks are generated on this card and are distributed.

18.3.3.2 Calibration Signal Generator – 3.2

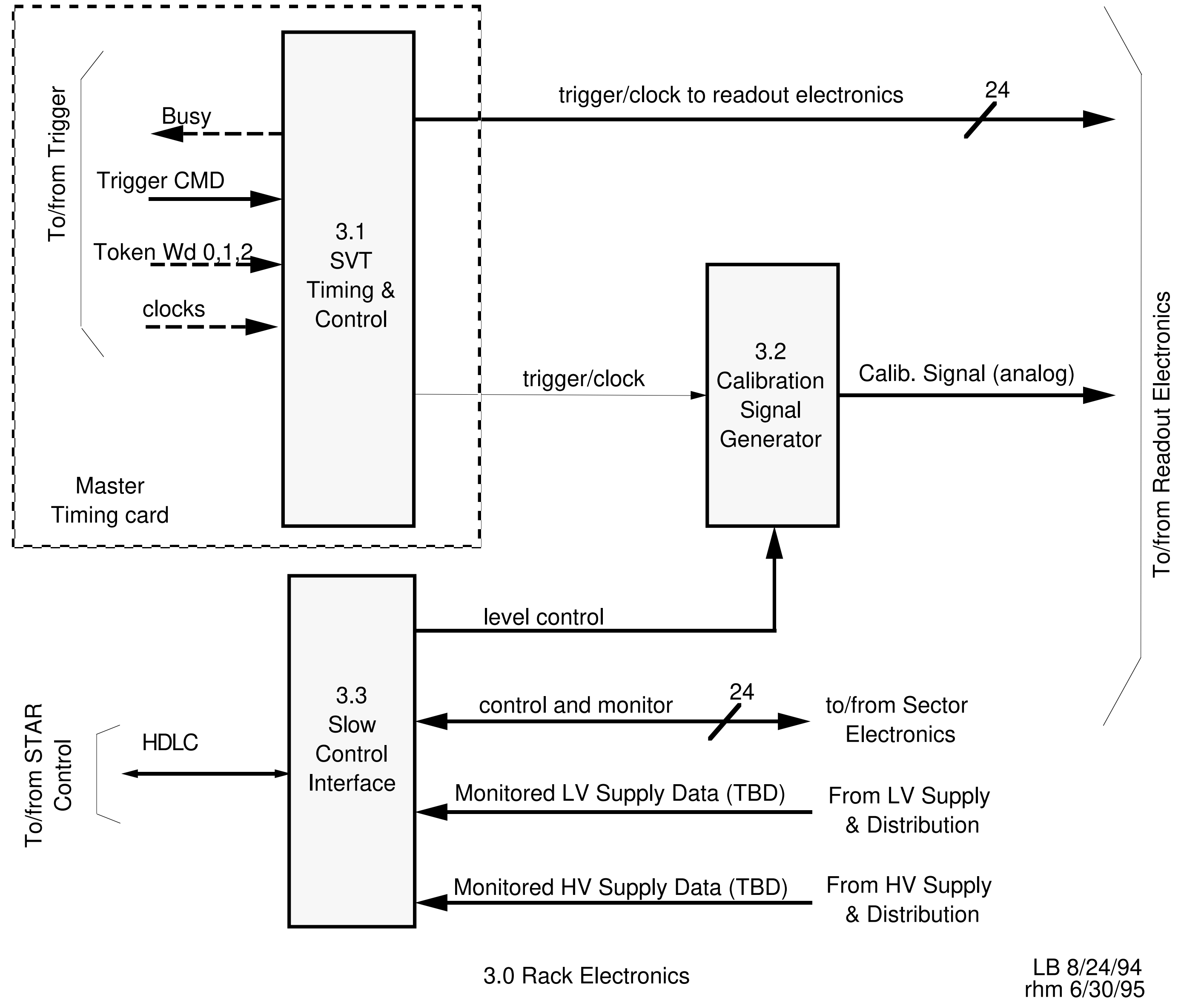
The calibration signal generator provides a variable voltage pulse (up to a few volts) to generate calibration pulses for SDD gain and offset calibration. The amplitude of the pulse is controlled via the Slow Control Interface. Timing of the pulse is from the Master Timing and Control Card. The output of the generator is masked via Controls to allow calibration of individual carriers. Individual SDDs are not accessible.

18.3.3.3 Slow Control Interface – 3.3

The Controls Interface is used for control and monitoring throughout the SVT. The HDLC link will be used for test data, all setup, and analog monitoring at the Sector Electronics. A commercial system will be used for power supply control and monitoring.

18.3.3.4 Power Systems – 4.0

Low Voltage (± 8 VDC will be provided by 24 supplies, each feeding one Sector readout module. High Voltage (-1500 V) will come from one Supply with multiple regulators to allow individual adjustment of HV. Steering Voltage (-100 V) will come from one supply with multiple regulators.


To/from Trigger
Busy
Trigger CMD
Token Wd 0,1,2
clocks
3.1
SVT
Timing &
Control
Master
Timing card
trigger/clock to readout electronics
24
trigger/clock
3.2
Calibration
Signal
Generator
Calib. Signal (analog)
To/from Readout Electronics
level control
3.3
Slow
Control
Interface
To/from STAR
Control
HDLC
control and monitor
24
to/from Sector
Electronics
Monitored LV Supply Data (TBD)
From LV Supply
& Distribution
Monitored HV Supply Data (TBD)
From HV Supply
& Distribution
3.0 Rack Electronics
LB 8/24/94
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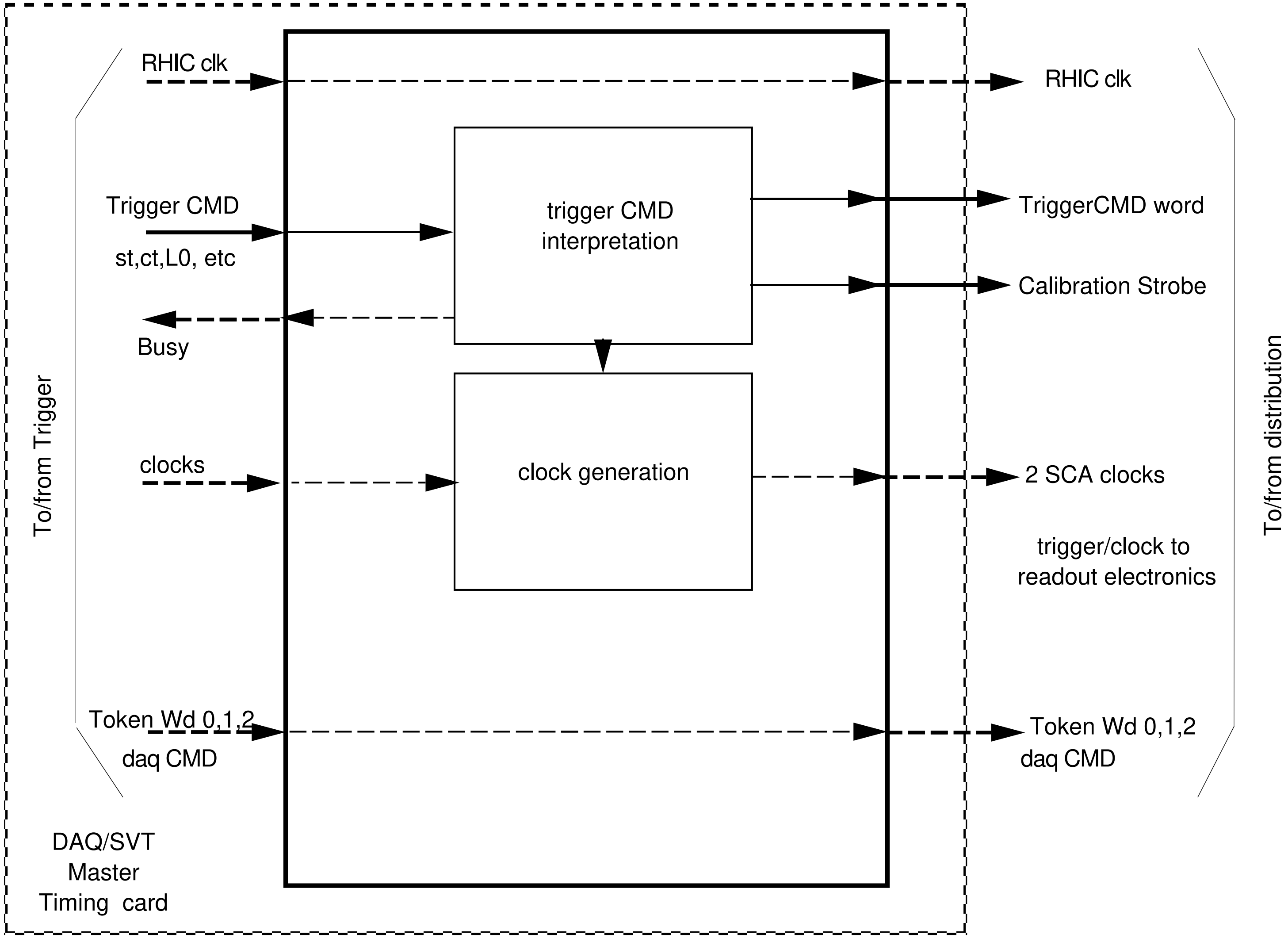

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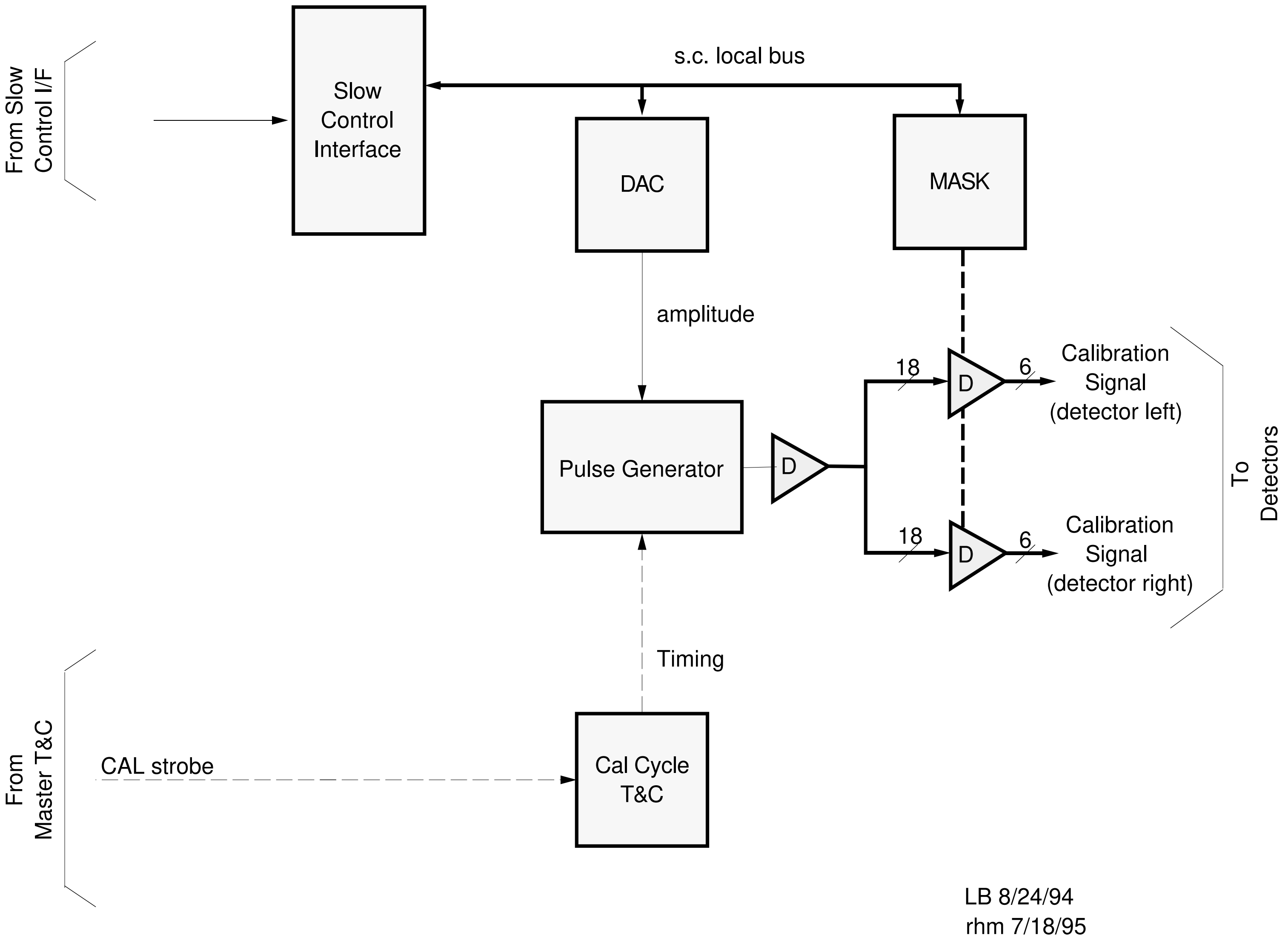
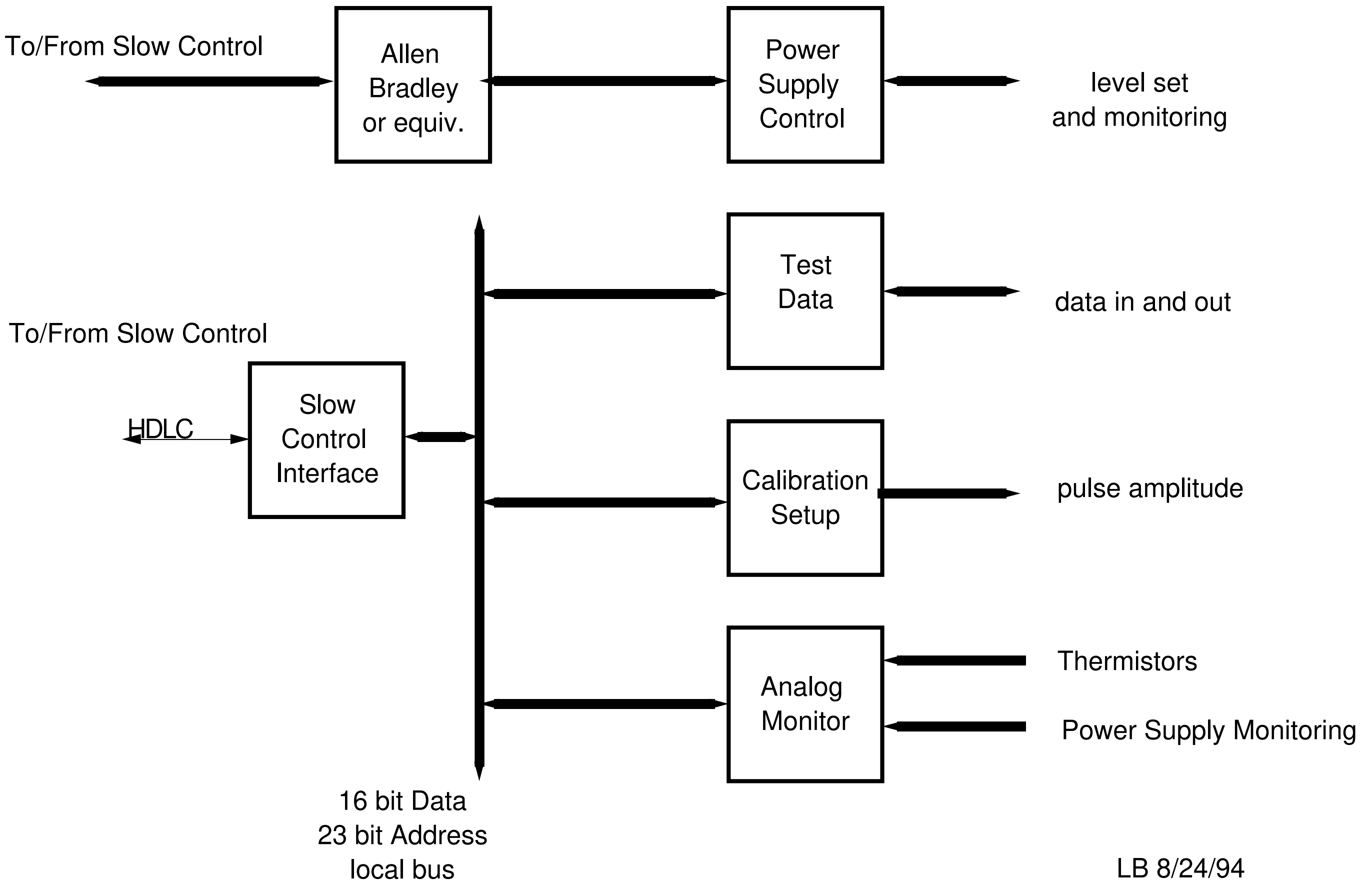
3.1 Master Timing and Control



3.2 Calibration Signal Generator (CSG)



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3.3 Slow Control Interface

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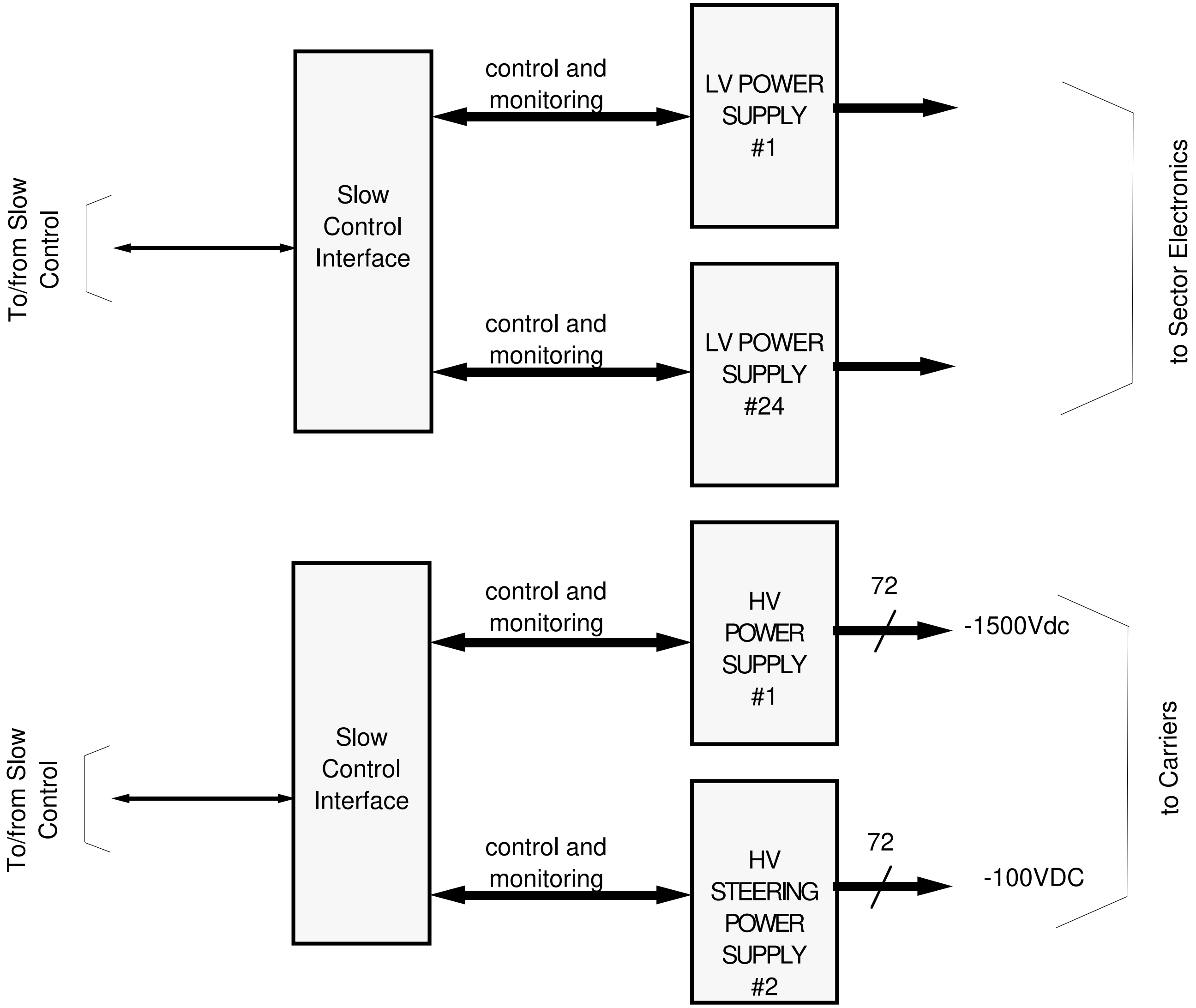

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4.0 Power Systems

Chapter 19

On-Line Software

Last Updated: 15 June 1995

This chapter contains essential model figures and words for on-line software.

Chapter 20

Off-Line Software

Last Updated: 15 June 1995

This chapter contains essential model figures and words for off-line software

Chapter 21

Infrastructure

Last Updated: 15 June 1995

This chapter contains essential model figures and words for software infrastructure.