Trigger Prototype Board

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1.0 Requirements

A minimal trigger circuit is needed for the SVT system test to drive the RDO electronics connected to the FEE. This trigger circuit needs to fulfill the following requirements:

- Provide an SCA acquisition clock of approximately 27 MHz.
- Provide an SCA readout clock of approximately 1 MHz.
- Provide a RHIC strobe for trigger synchronization of approximately 9 MHz.
- Provide at least one trigger data line strobe.
- Provide for an input level (NIM) to initiate a trigger.

The frequency requirements are guidelines which do not need to be fulfilled exactly. However, the actual provided frequencies should be as close as possible to the suggested values in order to test the RDO and FEE at conditions as close to the real ones as possible.

2.0 Proposed Design

Figure one shows our proposal for a prototype trigger board which fulfills the requirements stated above. The heart of the design contains a PLD which is responsible for generating all necessary clock outputs from a single 50 MHz oscillator. Additionally, it needs to provide a single pulse synchronized to the RHIC strobe in response to a high level input on the trigger input. In order to generate the SCA and RHIC clocks with the required asymmetry, the PLD first generates a 10 phase clock from the 50 MHz input in half-clock steps (10ns). The appropriate phases are then combined to generate a 25 MHz SCA acquisition clock (clock 1) with 10 ns low and 30 ns high. The RHIC strobe is generated as a 10 MHz pulse with 20 ns high. The RHIC strobe will also be connected as the DATAclk, even though this clock will not be used for anything for the system test. This provides the capabilities to extend the current design in the future. The SCA readout clock is generated from the RHIC strobe with a "divide-by-10", delivering a 1 MHz "clock 2". The trigger input level causes a one shot to fire in synch with the RHIC strobe. The output of the one-shot will serve as one of the 4 data bits, while the other 3 data bits are pulled to ground. The outputs of the PLD are connected to 2 ATT driver chips to provide the trigger interface signals required by the RDO electronics.

We propose to use a 6U-160 Vector prototyping board to house the circuitry. The logic required for this design can easily be implemented in an Altera EPM7032lc44-7 PLD. The drivers should be of the same type proposed for the STAR TCB boards (ATT 41MP - Quad differential drivers in DIP packages). The connector should be chosen to match the

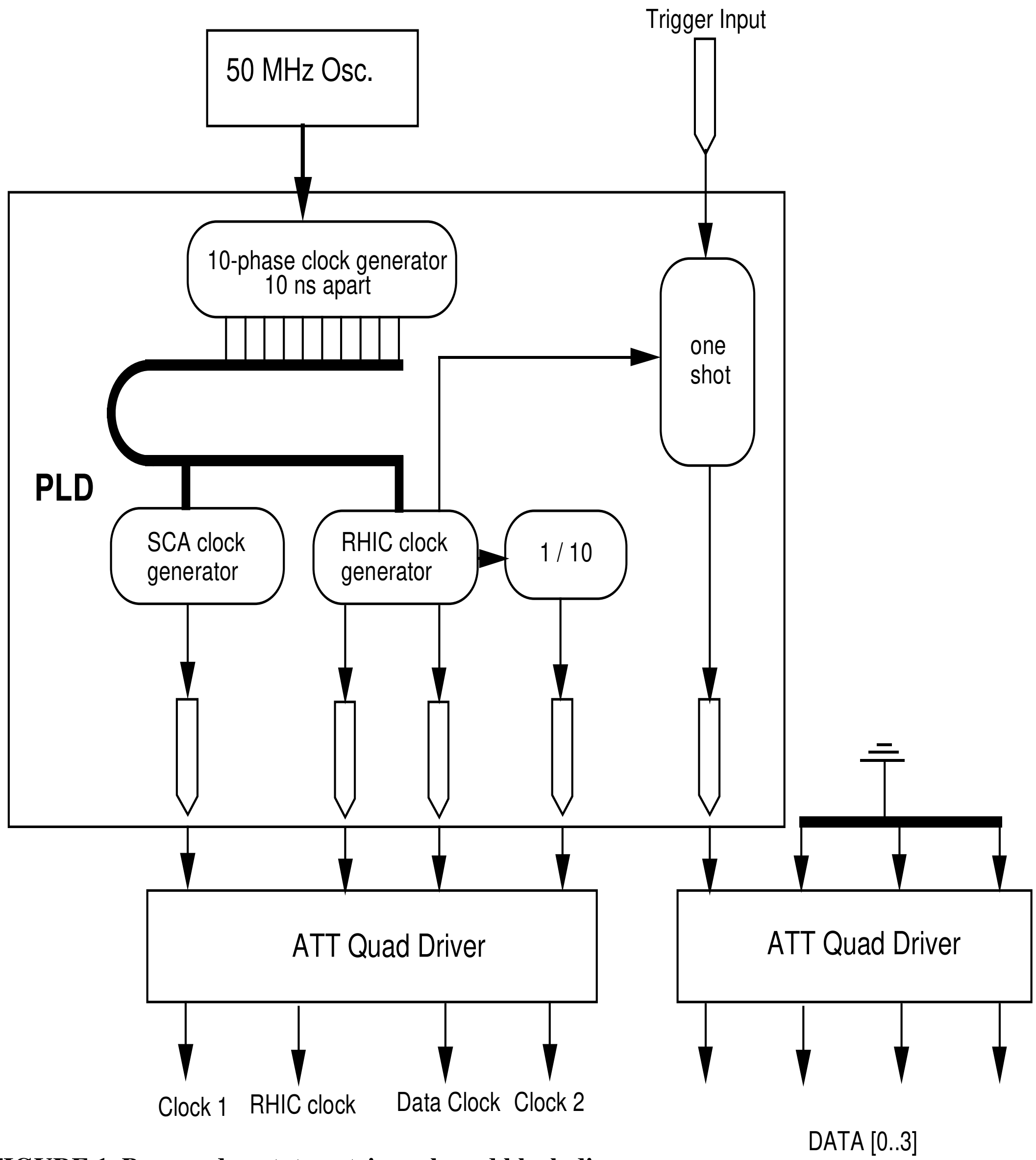

FIGURE 1. Proposed prototype trigger board block diagram.

RDO-PTB trigger input, i.e. use a 20-pin 3M IDC connector. The single 5V power required for this circuitry can be drawn from the VME rack.

3.0 Parts List for the proposed design

- 1 Vector E160-6U-1 prototyping board
- 1 Altera EPM7032LC44-7 PLD

- 1 Digi-Key A417-ND solder tail 44-pin PCC socket
- 1 50 MHz 4-pin oscillator
- 1 3M 3428-5002 20-pin IDC connector
- 2 ATT 41MP quad differential drivers
- 2 16-pin IC sockets
- 1 lemo input trigger connector