SVT Prototype Readout Electronics

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1.0 Introduction

A "System Test" is required to demonstrate that the proposed Silicon Vertex Tracker (SVT) for STAR is a technically feasible construction project and that its performance will meet design specifications. The "System" to be tested consists of a "ladder" (of the same mechanical structure as proposed for the STAR SVT) containing 7 Silicon Drift Detectors (SDD's) of the STAR2 design (bi-directional drift) and prototype electronics carriers, carrier interfaces, and front-end electronics.

Rather than build a custom readout system which only can be used for the System Test, it was decided to build a prototype of the proposed readout electronics for the SVT and to interface it to prototype data acquisition (DAQ) electronics currently being designed and constructed for a TPC system test in June 1995. The SVT System Test will occur at the end of 1995. The intent is that these SVT Readout Electronics serve as prototypes of the Readout Electronics of the final SVT system.

The University of Texas at Austin is responsible for designing and building the SVT Prototype Readout Electronics. This document presents the current status of the System Test requirements as discussed in the SVT group and a proposal for prototype readout electronics for the System Test.

2.0 The SVT System Test

The System will consist of the following parts:

- A mechanical structure (the ladder) which holds 7 SDD's and 2 electronics carriers.
- 7 SDD's of the STAR2 design, with 240 readout anodes on either side (480 readout anodes total on each detector)
- Front-End-Electronics Hybrids containing pre-amps, shaper-amps, and SCA's for analog sampling of the SDD's
- Carrier Interface Hybrids
- Prototype Readout Electronics
- Prototype DAQ Electronics (designed and constructed by the DAQ group)
- DAQ processors and tape storage for verification and processing of the data.

The proposed SVT contains three types of ladders which hold different numbers of SDD's. The largest ladders are located on the outer layer of the SVT, which each contain 7 SDD's. The construction of these ladders is one of the most challenging tasks from both

mechanical and electronics standpoints, so one of these ladders was chosen for the SVT System Test.

The front-end-electronics on each ladder are interfaced to the Readout Electronics at each end of the ladder via the Carrier Interfaces; each Readout Electronics system interfaces to 3 SVT ladders simultaneously, but no more than 3 1/2 detectors of an individual SVT ladder will be read out by one Readout Electronics system (see Essential Model of the SVT electronics). Therefore, it is sufficient to readout 4 of the 7 SDD's for the System Test.

The flow of data in an SVT ladder is as follows: Each SDD has 240 readout anodes on each end wirebonded to an FEE hybrid on the electronics carriers. The hybrids contain: 15 PASA (pre-amp-shaper-amp) chips each servicing 16 anodes; 15 SCA (switched capacitor array) chips with 16 channels each, sampling the output of the PASA into 128 (possibly 256) time samples for each channel; and hybrid I/O interfaces. For each hybrid the outputs of all SCA's are multiplexed onto one analog bus, which therefore carries the analog samples from 240 SDD channels. For the largest SVT ladder there are 14 analog lines, 7 on each carrier. For each carrier 4 analog lines go to one end of the electronics carrier, while the remaining 3 analog lines go to the other end of the carrier. Thus, the distribution of analog lines on the ladder is such that a total of 7 are connected to each end of the ladder (4 at one Carrier Interface and 3 at the other Carrier Interface). At either end of the electronics carriers a "Carrier Interface" hybrid will provide for the regeneration of the signals to be driven to the Readout Electronics. These interface hybrids will also contain receivers for the regeneration of digital control signals sent from the Readout Electronics to the FEE hybrids (mainly used for the control and timing of the SCA's). For the System Test 4 analog lines on each side of the detectors will be connected to one side of the ladder, for a total of 8 analog lines (from 4 detectors).

The readout electronics is responsible for the A/D conversion of the signals, intermediate buffering and possible storage of the converted data, and feeding the digital data via an optical fiber link (the HP Gigalink) to the DAQ electronics. In addition to this task, the readout electronics needs to provide regulated power to the FEE, provide timing and control signals for the SCA's on the hybrids, and provide an interface for the trigger and slow control systems. The readout electronics is described in more detail in the next section.

The DAQ electronics for the system test will consist of a commercial VME processor board by Cyclone Microsystems with an Intel 80960 (i960) processor, and a custom mezzanine board containing the HP Gigalink receiver, 2 Mb of VRAM, and control logic. This mezzanine card is currently being designed and constructed by the DAQ group at BNL as a custom "SQUALL" module, so that it can be connected and read out by the Cyclone board's i960. The i960 will appear as an intelligent peripheral to the VME system, so that it can be integrated into a VME DAQ system as a data source. A command interface to the Cyclone board is described in the document "DAQ temporary receiver card: Command/ Response definitions" by M. LeVine. We will write software for the System Test DAQ system (the Cyclone board and a Motorola VME processor). This software might incorporate some of the "miniDAQ" software developed for the TPC system test. The Cyclone board will not achieve the data throughput rates expected for the final DAQ Receiver boards, which need to receive up to 100 events/sec. This is due to the limited processor

power of the Cyclone board (one i960 instead of 18 ASIC's and 3 i960's). Therefore the expected data rate during the system test will be more in the order of a few events rather than the full 100 events/sec capability of the FEE. However, the higher rate is not required for the System Test, so a lower rate is acceptable.

3.0 Readout Electronics Requirements

The general philosophy guiding the design of the prototype readout electronics is to implement as much of the functionality of the final design as possible within the given budgetary and time constraints. Basic design requirements that can be deduced from the descriptions in the previous sections and the essential model documents are discussed below.

The readout card needs to be able to receive signals from 8 analog inputs and produce digitized values from the inputs. Currently, the system design plans digitization to 10 bits with an accuracy < 0.1% of the full scale (corresponding to 1 LSB for a 10 bit range). However, the readout electronics should provide for testing of several ADC designs in parallel. The readout electronics need to accept the analog signals at a rate up to 100 full events/sec.

The readout electronics need to provide the digitized data to the DAQ electronics via an HP Gigalink optical fiber connection in a protocol specified by the FEE <=> DAQ interface document: there will be two major blocks of data for each event, preceded by a command word and a 100 ns delay. The two data blocks are a 64 word header and an appropriately sized block of data, which has 2 ten-bit data values combined into 20-bit optical transmission words. The data transfer for each event finishes either with an "event abort" or an "event end" command (each followed by at least 100 ns of delay). The contents of the header is partially specified in the same interface document.

The readout electronics needs to provide an interface to the trigger system. This interface is specified in the Trigger => FEE interface document. The trigger interface also contains the interface for the clock distribution tree. As described in this document, the interface consists of a total of 8 signals/clocks: a RHIC clock strobe, 2 detector specific clocks, a data clock (running at 5 times the RHIC clock), and 4 bits of data. There are five 4-bit entities that are received and distributed for each trigger: a 4-bit trigger command (allowing for 16 different trigger actions by the readout electronics), a 4-bit DAQ command (only passed through to the event header), and a 12-bit trigger token (also passed through to the event header). The two detector specific clocks are the SCA read and write clocks. For the system test it is sufficient to implement 1 of the 16 trigger commands.

The readout electronics need to provide an interface to the slow controls system. Currently, the TPC group is designing a small daughter board (approximately 2.5" square) which presents the slow controls interface to a mother board as 24 address and 16 data lines, which can be memory mapped to appropriate actions on the mother board. The physical interface for slow controls is HDLC. The HDLC connector interface is presented on the daughter board connector, so that the mother board can have the actual HDLC con-

nector at a convenient place. The only slow controls function necessary for the system test is access to the event memory on the readout electronics, so that an event can be readout via slow controls, or a pattern can be downloaded to the event memory for testing of the fiber optics connection. However, it is desirable to provide for the readout of a thermistor on the SDD ladder and possibly a geometric ID of the electronics carrier via the slow controls. Both of these are required in the final system.

The readout electronics need to provide the clock and control signals for the SCA's on the hybrids. There are currently 5 of these signals:

- Clock: carries both the write (when data is sampled from the detectors) and read (when data is read from the SCA's to the readout electronics) clocks. The control sequencer on the readout electronics needs to connect the appropriate frequency to this line. Currently the write clock is 27 MHz and the read clock is 3 MHz. Both clocks are generated in the trigger control unit mezzanine card and provided to the readout electronics via the trigger interface.
- Read/Write select: This signal switches the mode of the SCA. The normal operation will have the SCA in write mode until a trigger is received (The SCA is free running, overwriting previous samples every 128/256 writes). When a trigger is received, the Write signal is released and read mode is initiated.
- Analog reset: This signal resets the analog bus. This should be done once for each time sample read. Since the readout sequence is such that a timesample is read out for all SCA's in the hybrid, before switching to the next time sample, the analog reset needs to be asserted every 240 reads (16 channels times 15 SCA's).
- Digital reset: This signal resets the pointers in the SCA's to a known value. This signal should be asserted before starting the sampling to have each SCA start sampling at the same cell.
- Token: This signal switches to the next time-sample and is passed from SCA to SCA. It should be asserted once every 240 reads.

These signals need to be driven 10 feet from the readout electronics to the carrier interface hybrids on the ladders.

The readout electronics need to provide clean power to the hybrids. The hybrids need +12, -12, +5, -5, +4, -2V. These voltages need to be generated and regulated by the readout electronics.

The readout electronics needs to provide for storage of one full event. This storage can either be filled by the A/D converters or via the slow controls link. The event in this storage area can be used as an alternative source for the fiber optic link. The data path will be controllable via slow controls.

4.0 Readout Electronics Implementation

Our proposal for prototype SVT readout electronics, illustrated in Fig. 1, uses three 6U-160 size VME boards shown as 3 functional blocks of the electronics. These 3 VME boards are the Power and Timing Board (PTB), the Analog input and buffer Memory Board (AMB), and the Fiber-Optic transmission Board (FOB). A short VME P2 backplane bus will be used as a 40-bit custom bus connecting these three boards.

The PTB interfaces to the trigger system, the slow controls system, and provides regulated power to both the other 2 readout electronics boards and the FEE. Central control for this board is an Altera PLD, which can implement the logic equations of the trigger receiver, and provide for the sequencing of the SCA timing and control. This PLD has connected to it receivers for the 8 trigger signals coming from the trigger system, and drivers for the clock and control signals to the SCA's on the FEE. The PLD allows easy reprogramming to adapt to changing requirements.

Power regulators receive raw power from an external power supply and provide regulated power at several levels to a front connector and the back plane for the other 2 boards.

A mezzanine slow controls board will be connected to the PTB via a 64 pin connector. This mezzanine board is currently under development by F. Bieser at LBL. The slow control EPROM will be customized for the readout application. Since slow controls can also be used to dump a whole event (the equivalent of the data from the 8 analog inputs) to the readout electronics, a transceiver will present this data to the backplane bus in 40-bit chunks. A stored event also can be read out via slow controls through this transceiver over the backplane. A slow instrumentation A/D will be provided for thermistor input to slow controls and the carrier ID will be able to be read if provided.

The tasks of the AMB are to receive the analog data from 8 hybrids, convert the analog samples to digital, provide buffering between the input frequency of the analog samples and the transmission frequency over the Gigalink fiber, and to provide possible storage for the digital data (to be loaded either from the ADC's or from the slow controls interface on the PTB). To provide for the difference in speed of the analog input and the Gigalink transmission frequency, the AMB stores all data in a 40-bit wide fast SRAM which acts as a buffer. The stored data can then be send at full speed to the FOB over the backplane in 40-bit chunks (presented by a 40-bit transceiver). This SRAM is also addressable over the backplane via a 20-bit address buffer. The timing and control of the AMB is done via an Altera PLD. The 8 ADC's of the AMB are read out by the AMB in two banks of 4 ADC's each. Current preference for the choice of these ADC's is the Analog Devices AD875, which can provide 10-bit data at 15 MHz and a precision of 0.4 LSB. However, several types of ADC's (probably 3 different ones) will be provided on the AMB. The parts for the current AMB design populate only about half of the real estate on a 6U VME board. However, we plan to implement the AMB as a full 6U board for possible extension to the full 18 analog channels required for the SVT readout electronics. It is possible to manufacture the AMB with traces for all 18 channels and only populate 8 of them for the system test.

The FOB contains the necessary parts for reading the digital data from the AMB in 40-bit chunks, convert them to the necessary level to present them to the HP Gigalink Transmitter in 20-bit words, and the fiber-optic transmitter laser diode (either from Finisar or from Methode). It will be necessary to test if the HP Gigalink transmitter can drive two photodiode transmitters, in case this kind of redundancy is desired for the final design. The FOB will provide space for two photodiodes, however, only one will be populated initially. Central timing and control is again achieved with an Altera PLD. The real estate needed for the parts of the FOB could fit on half of a 6U VME board, but for ease of handling a full 6U board will be used.

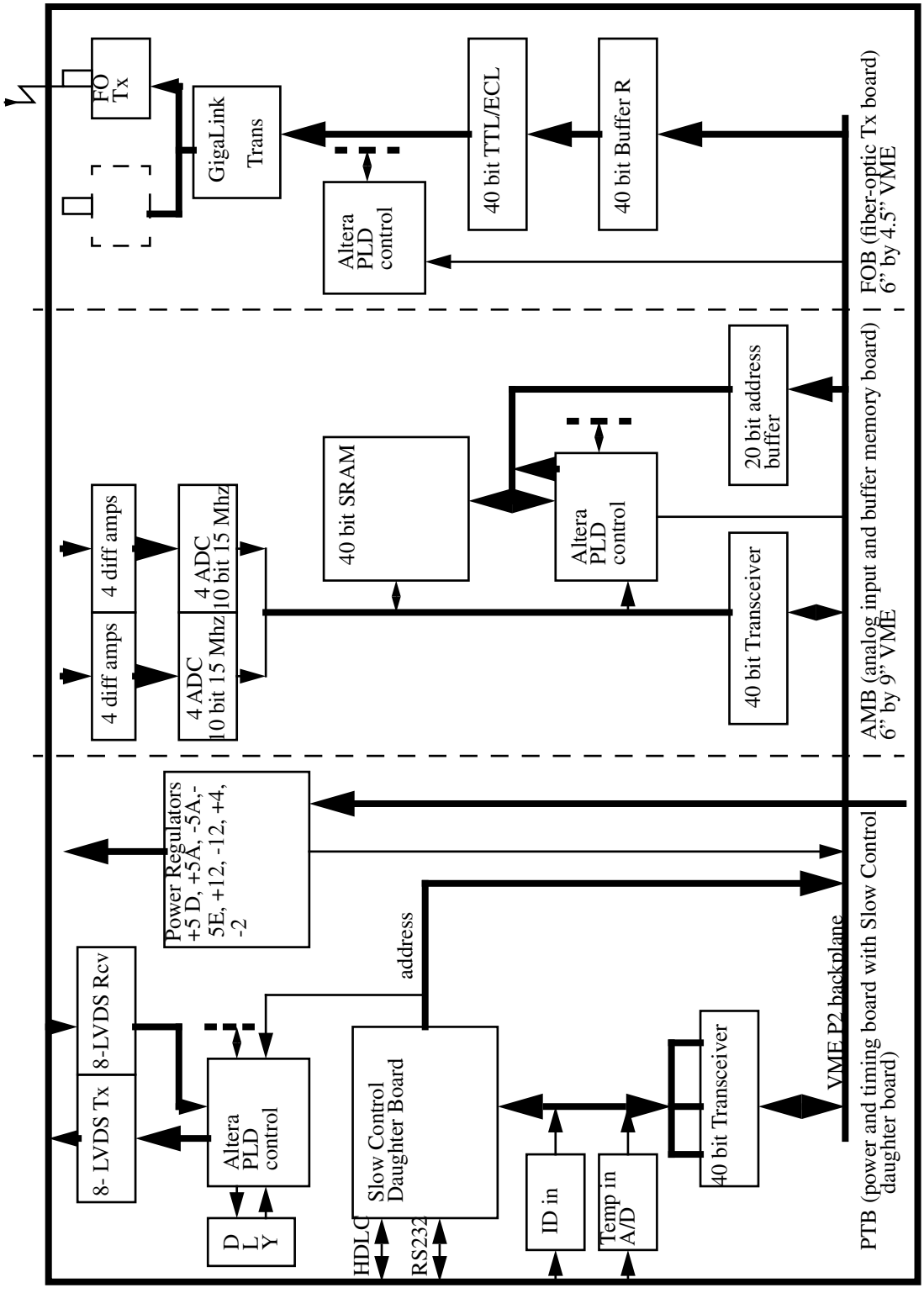

Fig 1: RO Prototype Block Diagram - Rev2 3/20/95 - GO