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SVT System Test Requirements Document

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Content:

1 Introduction

This is a Requirements Document for the *System Test* to be done for STAR's Silicon Vertex Tracker (SVT). Although the ultimate goal is a *System Test* of a complete *prototype* system, the most realistic approach is a **staged** approach in which the first **stage** demonstrates the proof of principle and subsequent **stages** lead to the final test of a complete *prototype* system. A successful **stage 1** is considered sufficient to extend SVT funding.

The main building blocks of the SVT system are:

- bidirectional Silicon Drift Detectors (**SDD**s) (240 readout anodes on either side, 480 readout anodes total on each detector)
- mechanical structures (**Ladders**) composed of **Detector Carriers** and **Electronics Carriers**
- Front-End-Electronics (**Hybrids**) made of preamplifiers – shaping amplifiers (PASAs), switch capacitor arrays (SCAs) , and multiplexing/control electronics
- **Carrier Interfaces** and associated **Carrier Interface Hybrids**
- High Voltage (**HV**) and distribution, Low Voltage (**LV**) and distribution
- **Readout Electronics**
- data acquisition (**DAQ**) receiver electronics
- **DAQ** processors, data analysis software, and data taping

The system test will include wafers glued to the detector carrier. The bias voltage will be delivered to the first wafer on a carrier and then daisy-chained across the ladder. The anodes of all detector will be wirebonded to the electronics carrier. The signals will be processed through hybrid prototypes fabricated on Beryllia substrate which will be glued onto the electronics carrier. The signals will be multiplexed in the SCA and forwarded into the ADC which resides on the off-detector readout electronics. The performance of this complete chain will be tested throughout the various stages of the system test.

2 Requirements Summary for the Stages of the System Test

The **requirements** associated with the various **stages** are summarized below. Details are given in later sections of this document.

2.1 Stage 1

[The main purpose is to demonstrate a working *prototype* of the proposed implementation of **Hybrid** electronics. These electronics contain PASAs (preamplifier and shaping amplifier), SCAs (switch capacitor array), and multiplexing/control electronics.]

time:

- Fabricate and test components by January 1996; do test of integrated system in February 1996.

  justification: the February 1996 date allows us to use the AGS proton beam running period for our beam tests. It also keeps the SVT project on the overall schedule towards a 1999 completion. We expect increased funding after the successful completion of the system test.

Silicon Drift Detectors:

- Use 4 **SDD**s of STAR2.7 or STAR2.8 prototype design.

  justification: STAR2.7 are the latest successful detector prototypes. It is the first batch with the final detector size. STAR2.8 will attempt to minimize the guard area even further. For the system test the STAR2.7 design is sufficient, because it could also serve as the final detector design. We decided to optimize the number of wafers for the system test to a.) show that an integrated system can work up to specification and b.) keep the number of 'wasted' wafers down. We do not expect to be able to 'recycle' system test wafers for the final SVT. The attachment to the Al ladders will make a disassembly impossible.

Ladders:

- Make all **Carrier** components out of aluminum. [If beryllium components are available, use them if possible.]

  justification: the procurement of Beryllium prototypes is under way. To minimize the cost of the support structure, foreign vendors might be used. In this case the delivery schedule for Beryllium parts might slightly shift. We expect the prototype pieces to be manufactured by the same vendor than the final structure. For stage 1 of the system test no mechanical tests are required. Therefore an Aluminum ladder will be used to replace non available Beryllium parts.

- Glue the **SDD**s to the **Detector Carrier**.

  justification: the gluing of the wafers to the carrier is one of the key feasibility tests. We might use different glues to compare and optimize the procedure. This step will be identical to the process used in the final design.

Front End Electronics:

- Use **Hybrid**s made from available SVT-SCA and SVT-PASA dies.

  justification: the submission available at the time of the system test should be sufficiently close to the final dies. We expect to use chips from the 3rd SCA submission and the 1st PASA submission.

- Fabricate **Hybrid**s on a Beryllia substrate and glue the substrate to the **Electronics Carrier**.

  justification: the hybrid production is a key element of a successful system test. The feasibility of the present hybrid design and its integration has to be proven. The gluing of the hybrid to the electronics carrier will correspond to the procedure foreseen for the final system.

- Keep the **Hybrid** width to within 30% of final requirement (max.= 2.5cm).

  justification: the early IC prototypes have a larger 'footprint' than the final designs. Although the spacing between channels (= 250 μm) is the same in every batch, the prototype batches result in a SCA of 4.8 $\times$ 4.8 mm^2, whereas the production batch give dies of 3.6 $\times$ 2.5 mm^2. That is due to the specific process MOSIS uses for prototyping. We might have to use the slightly larger dies for the system test. Also, the relative distance between PASA and SCA has to be optimized based on the cross talk characteristics. In the first stage we also consider surface mounted pods for the control logic in order to optimize the layout and the performance characteristics. In the final stage these components will be part of the substrate.

Carrier Interfaces/Interface Electronics:

- Impose no requirements for the **Carrier Interface**. Impose no requirements for cables or connectors.

  justification: the carrier interface as well as the cable connections are still under design. The layout of the carrier interface depends strongly on the test results from the cooling system prototype, because the water in- and outlets are part of the carrier interface. The remaining area has to be optimized for the various cable interfaces. Several connectors are being considered. Radiation length and maintainability studies are under way. The availability of connectors and past experience in other micro vertex detector projects shows that this part of the system test is not on a critical path, though.

High Voltage/Low Voltage:

- Impose no requirements for the **HV** power supplies and the **LV** power supplies. Impose no requirements for cables or connectors.

  justification: the voltage power supplies are standard. In particular the LV supplies will be identical to the TPC supplies. HV connectors are available, but a detailed safety study has to be performed for the various options. None of these items is on a critical path.

Readout Electronics:

- Use preliminary *prototype* **Readout Electronics**. Impose no requirements for cables or connectors.

  justification: the readout electronics are an off-detector item. They will be designed independently of the on-detector components. Most of the required parts are commercially available. Therefore the RDO is not on a critical path.

Data Acquisition:

- Use a VME based data acquisition (**DAQ**) system that receives digital data from the **Readout Electronics**.

  justification: the DAQ is based on the STAR-TPC system test DAQ.

- Use a **DAQ** that contains a VME processor for monitoring/on-line analysis and a tape drive for storing data.

  justification: the offline data processing is based on hardware and software used by NA49 and in previous SVT beam tests.

Performance:

- Achieve a Signal to Noise ratio of the complete chain that is within factor of 2 of final requirement (<800 *rms* electrons).

  justification: past experience with the TPC-SCA and TPC-PASA has shown that early submissions tend to exhibit noise problems. The optimization of the signal-to-noise ratio versus the power consumption and speed is a standard procedure in multiple submission cycles. The factor 2 requirement is based on the TPC experience and results from the first SCA submission.

2.2 Stage 2

time:

- by June 1996

test:

- **Stage 1** and a beryllium carrier for the **SDD**s.

2.3 Stage 3

time:

- by June 1996

test:

- **Stage 2** and a beryllium carrier for the **Hybrids** plus a prototype for the signal cable and connector interface

2.4 Stage 4

time:

- by September 1996.

test:

- **Stage 3** and **Hybrids** that meet final space requirements

2.5 Stage 5

time:

- by September 1996

test:

- **Stage 4** and achieve the required Signal to Noise ratio for the SVT; plus the final cable and connector design for the electronics carrier

2.6 Stage 6

time:

- by September 1996.

test:

- **Stage 5** plus *prototype* **Carrier Interfaces** and *prototype* **HV** and **LV** systems including prototype voltage cable and connector interface.

2.7 Stage 7

time:

- by December 1996.

test:

- **Stage 6** plus **Hybrids** made with final SCA and PASA dies, and 7 **SDD**s of the final design mounted on an outer **Ladder**

3 Details of System Test Components

This section specifies, for each component needed for the *System Test*:

- hardware **requirements**
- **justification** of **requirements**
- **description of hardware**
- **description of integration**
- **test plans** before *System Test*
- **personnel** assigned to task
- **timelines** for task completion

3.1 Silicon Drift Detectors (SDDs)

requirements: 4 STAR2.7 **SDD**s or 4 special STAR2.8 **SDD**s. Operating voltage must be at least 1500 V. SDD drift nonlinearity must contribute less less than 30 μm to the position resolution in drift and lateral direction. The linearity of the potential gradient as generated by external and internal resistor must be better than 5% of the individual bias level. The noise level introduced into the **SDD**s by external sources must be less than 20% of the total noise of the system (including electronics). The SDD itself must not introduce more than 10% of the total noise of the system.

justification: The **Readout Electronics** system for the SVT is such that no more than 4 detectors of an individual SVT **Ladder** will be read out by one **Readout Electronics** system (see Essential Model of the SVT electronics). Therefore, it is sufficient to readout 4 **SDD**s for the *System Test*. The testing of STAR2 and STAR2.5 detectors showed that the voltage breakdown, leakage current, and differential non-linearity characteristics do not meet all the design requirements for a final **SDD** batch. Subsequently a new version, STAR2.7 was designed, including all the specifications based on the the testing of the previous batches. If STAR2.7 is successful, it will be used for the *System Test*. If not, a STAR2.8 will be designed based on the results of the STAR2.7 tests. The decision concerning STAR2.7 versus STAR2.8 will be made by August 95.

description of hardware: The main changes for STAR2.7 are:

- increased detector size from 6 cm $\times$ 6 cm to 6.3 cm $\times$ 6.3 cm
- new shape and arrangement of guard structure to minimize inactive area
- increased anode bond pad size

- increased resistance in internal resistor chain to lower heat dissipation, and new resistor geometry (shape and length) to improve stability
- improved layout of guard structure to avoid early HV breakdown
- separation of first and last HV bond pads of less than 57 cm to allow usage of a groove-less detector carrier

description of integration: The detectors will be glued to the **Detector Carrier** and wirebonded to the **Electronics Carrier**. All 480 channels on each wafer will be bonded. HV will be provided to the first wafer and then daisy-chained to all detectors on the **Ladder**. HV will be supplied to the **Ladder** at one end only. The HV divider board is not part of the *System Test*. A standard size divider board (similar to those presently used in the laboratories) will supply the voltages to the first wafer via ribbon cable. A standard connector (not the final version) will be used at the **Ladder**. The anodes will not be bonded directly to the PASA but rather to a bond pad on the **hybrid** using a special jig.

test plan: The tests planned for both STAR2.7 and STAR2.8 include:

- bonding studies with bare silicon pieces and an aluminum **Detector Carrier**
- leakage and surface current studies
- HV breakdown studies
- drift linearity studies
- shielding and grounding studies
- noise source studies

personnel:

coordinator: Hobie Kraner (BNL)

SDD design: Lie Dou (WSU), Gintas Vilkelis (OSU), Hobie Kraner (BNL)
production: Lie Dou (WSU), Josef Sedlmeir, Wei Chen (BNL)
mounting: Rolf Beuttenmueller (BNL), Hobie Kraner (BNL)
testing: Josef Sedlmeir (BNL), Jerry Hall (WSU), Al French (WSU), Gintas Vilkelis (OSU), Ivan Kotov (OSU)

timelines:

Table 1 gives the timelines for **SDD** tasks.

Task	**Start Date**	**Completion Date**
build STAR2.7		June 1995
test STAR2.7		August 1995
build STAR2.8		September 1995
test STAR2.8		December 1995

Table 1: Timelines for **SDD** construction

3.2 Detector and Electronics Carriers

requirements: One **Ladder** made from aluminum of same mechanical design as proposed SVT **Ladder** (made of beryllium).

justification: The **SDDs**, the **Hybrids**, and the associated **multiplexing/control electronics** are mounted on the **Ladder**.

description of hardware: A *prototype* aluminum **Ladder** will be built in the U.S. [A beryllium prototype will be made by a Russian vendor and used for subsequent stages of the *System Test*. If the Russian vendor delivers prototypes in 1995, beryllium carriers will be used in **Stage 1** as well.] Since the outer carrier holds 7 detectors while the inner carrier holds 4 detectors, the inner carrier must have increased structural rigidity. For **Stage 1** we will use an inner layer **Detector Carrier**.

A complete **Ladder** consists of several independent parts:

- 1 **Detector Carrier**
- 2 **Electronics Carriers**
- angle brackets for connecting **Electronics Carriers** to **Detector Carrier**

The various **Ladder** parts have been designed and are described in the SVT hardware document section on the WorldWideWeb. CAD drawings, specifying the exact dimensions including tolerances are found in this section as well. The prototype pieces will be manufactured according to drawings:

- SVT001 [Layer 1(out of 6 layers = 3 superlayers)]
- SVT010 (detector assembly; incl.drawings: SVT028,SVT031-032,SVT035)
- SVT022 (electronics assembly; incl.: SVT038-044)
- SVT045 (PIN)

- SVT046 (HV connector)
- SVT047 (hybrid board connector)

description of integration: Special jigs will allow assembly of the three (3) independent pieces. However, for **Stage 1** of the *System Test* no angle mount of the **Electronics Carriers** is required.

test plan: The tests will include investigation of:

- mechanical stability versus water throughput
- temperature gradient measurement using present cooling scheme
- mechanical stability versus air flow
- mechanical stability versus cable load
- pressure drop versus water flow rate
- evaluation of galvanization effect of materials in water
- mechanical structure static deformation due to weight

personnel:

coordinator: Chong-Jer Liaw (BNL)

Ladder design: Chong-Jer Liaw (BNL), John Dioguardi (BNL)
production: Russia or U. S. Vendor
detector mounting: Chong-Jer Liaw (BNL), Hobie Kraner (BNL)
electronics mounting: David Lynn (BNL), Siegfried Hart (WSU)
testing: Chong-Jer Liaw (BNL), John Dioguardi (BNL), David Lynn (BNL)

timelines:

Table 2 gives the timelines for **Ladder** tasks.

Task	Start Date	Completion Date
Al Carrier production		June 1995
test setup design		June 1995
test setup assembly		August 1995
Al Carrier assembly		August 1995
Ladder testing		October 1995
Be Carrier production		October 1995
Be Carrier assembly		December 1995

Table 2: Timelines for **Ladder** work

3.3 Front-End-Electronics Hybrids

requirements: Eight (8) **Hybrids** mounted on a **Carrier**. Tracelines and additional control logic on the **Carrier**.

PASA dynamic range, linearity and noise must satisfy the requirements stated in the SVT-FEE requirements document. SCA dynamic range, linearity, noise, pedestal and token function must satisfy the requirements stated in the SVT-FEE requirements document. The analog multiplexing stage must operate at a readout rate of at least 3.3 MHz. The **Hybrid** packaging density must satisfy the **Hybrid** space requirements as stated in the SVT-FEE requirements document. The **Hybrid** has to meet the power consumption requirements stated in the SVT-FEE requirements document.

justification: Front-End-Electronics (FEE) (Hybrids) (containing preamplifiers, shaping amplifiers, switch capacitor arrays, control logic, buffers, and drivers) generate **SDD** analog signals for the **Readout Electronics**.

Each **SDD** has 240 readout anodes on each end wirebonded to an **FEE Hybrid** on the **Electronics Carriers**. The **Hybrids** contain: 15 PASA (pre-amp-shaper-amp) chips [each servicing 16 anodes]; 15 SCA (switched capacitor array) chips [16 channels each], sampling the output of the PASA into 128 (possibly 256) time samples for each channel; and **Hybrid** I/O interfaces. For the SVT, each **Readout Electronics** system interfaces to 3 **Ladder**s simultaneously, but no more than 4 detectors of an individual **Ladder** will be read out by one **Readout Electronics** system (see Essential Model of the SVT electronics). Therefore, it is sufficient to readout 4 **SDD**s for the *System Test*. Since each **Hybrid** interfaces to 1/2 of an **SDD**, eight (8) are required.

description of hardware: The PASA will be either a bipolar or CMOS bare die (16 channels). The SCA will be a CMOS bare die (16 or 24 channels). The requirements for both chips are specified in the SVT electronics requirements document, located in the SVT hardware document section on the WorldWideWeb. Depending upon the SCA design, the driver/buffer will be located either at the **Hybrid** I/O or at the **Carrier Interface** I/O. The driver/buffer will have full driving capability (at least 3 m). In addition to the two main integrated circuits and the driver amplifier, multiplexing electronics and control logic will reside on the **Hybrid**. Hopefully the **Hybrid** prototype design will allow the **Electronics Carrier** for **Stage 1** to be the 2 cm $\times$ 56 cm size required by the SVT design, but this is not a requirement until **Stage 4**.

description of integration: A detailed **Hybrid** layout will be made. This layout will specify also the remaining on-**Hybrid** electronics. The PASA and SCA dies will be integrated in a Beryllia substrate, all other components will be surface mounted to the Beryllia. The final Beryllia part will be glued to the **Electronics Carrier**.

test plan: The tests planned include investigation of:

- token passing readout functionality as a function of clock rate
- write data cycles as a function of clock rate
- read data cycle as a function of clock rate
- power consumption in write mode vs speed
- power consumption in read mode vs speed
- power consumption in standby
- pedestal variation
- first cell discontinuity
- input/output capacitance
- noise
- verify 100μs pause effects
- functionality of all secondary components (multiplexer, control logic)
- mechanical stability of mounted and glued **Hybrid**
- ruggedness of bonded wires
- maintainability and repairability of mounted and glued **Hybrid**

personnel:

coordinator: David Lynn (BNL)

PASA design and testing: Don DiMassimo (BNL), Paul O'Connor (BNL), Siegfried Hart (WSU)
SCA design and testing: Stuart Kleinfelder (LBL), Bob Minor (LBL)
hybrid component selection: David Lynn (BNL), Bob Minor (LBL)
hybrid design: David Lynn (BNL), Don DiMassimo (BNL), Dimitri Stephanie (BNL)
production: U.S. Commercial Vendor
testing: David Lynn (BNL), Siegfried Hart (WSU)
mounting: David Lynn (BNL), Chong-Jer Liaw (BNL)

timelines:
Table 3 gives the timelines for **Hybrid** tasks.

Task	Start Date	Completion Date
Hybrid specification document		June 1995
Hybrid component selection		June 1995
SCA prototype (tested)		July 1995
PASA prototype (tested)		July 1995
Hybrid layout		August 1995
Hybrid prototype		September 1995
Hybrid submission		October 1995
Hybrid testing		December 1995
Hybrid mounting		January 1996

Table 3: Timelines for **Hybrid** work

3.4 Carrier Interfaces

requirements: Two (2) **Carrier Interfaces**.

justification: At each end of the **Ladder** the **Front-End-Electronics** are interfaced to the **Readout Electronics** via the **Carrier Interfaces**. A maximum of 4 **SDD** analog lines pass through a given interface to the **Readout Electronics**. Since the *System Test* will involve just 4 **SDD**s, only two **Carrier Interfaces** (both on same side of **Ladder**) are required for the 8 **Hybrids**.

A **Carrier Interface Hybrid** has to regenerate the signals to be driven to the **Readout Electronics**. These **Carrier Interface Hybrids** will also contain receivers for the regeneration of digital control signals sent from the **Readout Electronics** to the **FEE Hybrids** (mainly used for the control and timing of the SCAs).

description of hardware: The final **Carrier Interface** has to satisfy SVT layout and space requirements (10 cm $\times$ 2 cm). However, for the *System Test* a larger PC board version can be used. The final version of the **Carrier Interface** will not be prototyped by the end of 1995, so the *System Test Carrier Interface* will consist of the following parts:

- a standard PC board that attaches either to the end of the **Ladder**, or resides in a VME crate
- drivers for analog signals
- I/O logic
- monitoring/slow controls logic
- power distribution logic
- water cooling inlet/outlet

The various components all commercially available. A Requirements Document containing a layout design and a detailed parts list must be prepared.

description of integration: The **Carrier Interface** for the first **stages** of the *System Test* will reside on a PC board and connect to the **Electronics Carrier** via a cable/connector interface.

The final **Carrier Interface** is under design. Presently an extension of the **Electronics Carrier** with the dimensions of 10 by 2 cm is envisioned. It will contain the **Carrier Interface** as well as the water in- and outlets, plus the signal, control cable and low voltage connectors. A prototype will be mounted to the extension of the **Electronics Carrier** in the same fashion the **Hybrid** Beryllia substrate gets mounted to the **ΠElectronics Carrier**. Both parts will be glued to the carrier.

test plan: (for *prototype or final* **Carrier Interface**)

- write data cycles as a function of clock rate
- read data cycle as a function of clock rate
- power consumption in write mode as a function of clock speed
- power consumption in read mode as a function of clock speed
- power consumption in standby
- multiplexing functionality
- noise
- mechanical stability of mounted and glued **Carrier Interface**

- ruggedness of bonded wires
- maintainability and repairability of mounted and glued **Carrier Interface**

personnel:

coordinator: David Lynn (BNL), Bob Minor (LBL)

design and component selection: David Lynn (BNL), Bob Minor (LBL)
production: Brookhaven National Laboratory
testing: David Lynn (BNL), Siegfried Hart (WSU)
mounting: David Lynn (BNL), Chong-Jer Liaw (BNL)

timelines:
Table 4 gives the timelines for **Carrier Interface** tasks.

Task	Start Date	Completion Date
design of **Carrier interface** PC board version		July 1995
test of **Carrier interface** PC board version		December 1995
final **Carrier Interface** component selection		September 1995
final **Carrier Interface** design		October 1995
final **Carrier Interface** prototype		December 1995
final **Carrier Interface** testing		February 1996
final **Carrier Interface** mounting		April 1996

Table 4: Timelines for **Carrier Interface** work

3.5 High Voltage and Low Voltage Power Supplies

requirements: A negative high voltage **Power Supply** (variable to -2500 V) and + 24V, +/-16V, +/- 5 V, and +/- 2 **Power Supplies**.

justification: The **SDD**s require negative high voltage. The **Readout Electronics** and **Hybrids** require low voltage.

description of hardware: For the SVT, the HV and LV supplies most likely will be commercially available power supplies. The features will be comparable to those of supplies presently in use in the SVT test laboratories.

description of integration: All power supplies will be located in a crate near the **Ladder** and **Readout Electronics**. LV supply cables will be interfaced with the **Electronics Carriers**. A HV line will connect to an external voltage divider board located in a crate near the **Ladder**. The board will supply 50 voltages to the first detector on a detector **Ladder**. On the **Ladder** the HV will be daisy-chained from wafer to wafer. HV will be supplied to both sides of a wafer and from both sides of a **Ladder**.

During the early **stages** of the *System Test* standard HV cables and connectors will be used.

test plan:

- test the LV connection to the **Electronics Carrier**
- test the HV connection to the first wafer on a **Ladder**
- test the daisy-chain across the **Ladder**

personnel:

coordinator: David Lynn (BNL)

Power Supply selection: Jerry Hall (WSU), David Lynn (BNL)
connectors, cables, daisy-chaining: Bob Minor (LBL), David Lynn (BNL)
testing: Siegfried Hart (WSU), David Lynn (BNL)

timelines:

Table 5 gives the timelines for **Power Supply** tasks.

Task	Start Date	Completion Date
select **Power Supplies**		July 1995
test **Power Supplies**		August 1995
test **Power Supply Integration**		December 1995

Table 5: Timelines for **Power Supply** tasks

3.6 SVT Prototype Readout Electronics

requirements: A prototype **Readout Electronics** system to take data from the detector, digitize it, and send it to **DAQ** electronics.

justification: The **Readout Electronics** is responsible for removing the data from the detector, the A/D conversion of the signals, intermediate buffering and possible storage of the converted data, and feeding the digital data via an optical fiber link (the HP Gigalink) to the DAQ electronics. In addition to this task, the **Readout Electronics** provides regulated power to the **FEE**, provides timing and control signals for the SCAs on the **hybrids**, and provides an interface for the trigger and slow control systems.

description of hardware: The general philosophy guiding the design of the prototype readout electronics is to implement as much of the functionality of the final design as possible within the given budgetary and time constraints. Basic design requirements that can be deduced from the descriptions in the previous sections and the essential model documents are discussed below.

The readout card needs to be able to receive signals from 8 analog inputs and produce digitized values from the inputs. Currently, the system design plans digitization to 10 bits with an accuracy $< 0.1\%$ of the full scale (corresponding to 1 LSB for a 10 bit range). However, the **Readout Electronics** should provide for testing of several ADC designs in parallel. The **Readout Electronics** need to accept the analog signals at a rate up to 100 full events/sec.

The **Readout Electronics** need to provide the digitized data to the DAQ electronics via an HP Gigalink optical fiber connection in a protocol specified by the **FEE** — **DAQ** interface document: there will be two major blocks of data for each event, preceded by a command word and a 100 ns delay. The two data blocks are a 64 word header and an appropriately sized block of data, which has 2 ten-bit data values combined into 20-bit optical transmission words. The data transfer for each event finishes either with an event abort or an event end command (each followed by at least 100 ns of delay). The contents of the header is partially specified in the same interface document.

The **Readout Electronics** needs to provide an interface to the trigger system. This interface is specified in the Trigger $\rightarrow$ **FEE** interface document. The trigger interface also contains the interface for the clock distribution tree. As described in this document, the interface consists of a total of 8 signals/clocks: a RHIC clock strobe, 2 detector specific clocks, a data clock (running at 5 times the RHIC clock), and 4 bits of data. There are five 4-bit entities that are received and distributed for each trigger: a 4-bit trigger command (allowing for 16 different trigger actions by the **Readout Electronics**), a 4-bit DAQ command (only passed through to the event header), and a 12-bit trigger token (also passed through to the event header). The two detector specific clocks are the SCA read and write clocks. For the *System Test* it is sufficient to implement 1 of the 16 trigger commands.

The **Readout Electronics** need to provide an interface to the slow controls system. Currently, the TPC group is designing a small daughter board (approximately

2.5 square) which presents the slow controls interface to a mother board as 24 address and 16 data lines, which can be memory mapped to appropriate actions on the mother board. The physical interface for slow controls is HDLC. The HDLC connector interface is presented on the daughter board connector, so that the mother board can have the actual HDLC connector at a convenient place. The only slow controls function necessary for the *System Test* is access to the event memory on the **Readout Electronics**, so that an event can be readout via slow controls, or a pattern can be downloaded to the event memory for testing of the fiber optics connection. However, it is desirable to provide for the readout of a thermistor on the **SDD** and/or the **Electronics Carrier** and possibly a geometric ID of the **Electronics Carrier** via the slow controls. Both of these are required in the final system. The **Readout Electronics** need to provide the clock and control signals for the SCAs on the **Hybrids**. There are currently 5 of these signals:

- Clock: carries both the write (when data is sampled from the detectors) and read (when data is read from the SCAs to the **Readout Electronics**) clocks. The control sequencer on the **Readout Electronics** needs to connect the appropriate frequency to this line. Currently the write clock is 27 MHz and the read clock is 3 MHz. Both clocks are generated in the trigger control unit mezzanine card and provided to the **Readout Electronics** via the trigger interface.

- Read/Write select: This signal switches the mode of the SCA. The normal operation will have the SCA in write mode until a trigger is received (The SCA is free running, overwriting previous samples every 128/256 writes). When a trigger is received, the Write signal is released and read mode is initiated.

- Analog reset: This signal resets the analog bus. This should be done once for each time sample read. Since the readout sequence is such that a timesample is read out for all SCAs in the **Hybrid**, before switching to the next time sample, the analog reset needs to be asserted every 240 reads (16 channels times 15 SCAs).

- Digital reset: This signal resets the pointers in the SCAs to a known value. This signal should be asserted before starting the sampling to have each SCA start sampling at the same cell.

- Token: This signal switches to the next time-sample and is passed from SCA to SCA. It should be asserted once every 240 reads.

These signals need to be driven 10 feet from the readout electronics to the **Carrier Interface Hybrids** on the **Ladder**s.

The **Readout Electronics** need to provide clean power to the **Hybrids**. The **Hybrids** need +12, -12, +5, -5, +4, -2V.

These voltages need to be generated and regulated by the **Readout Electronics**.

The **Readout Electronics** needs to provide for storage of one full event. This storage can either be filled by the A/D converters or via the slow controls link. The event in this storage area can be used as an alternative source for the fiber optic link. The data path will be controllable via slow controls.

description of integration: Our proposal for prototype SVT **Readout Electronics**, uses three 6U-160 size VME boards. These 3 VME boards are the Power and Timing Board (PTB), the Analog input and buffer Memory Board (AMB), and the Fiber-Optic transmission Board (FOB). A short VME P2 backplane bus will be used as a 40-bit custom bus connecting these three boards. The system is described in detail in the RDO Electronics document on the WorldWide Web under SVT hardware documents.

The PTB interfaces to the trigger system, the slow controls system, and provides regulated power to both the other 2 **Readout Electronics** boards and the **FEE**. Central control for this board is an Altera PLD, which can implement the logic equations of the trigger receiver, and provide for the sequencing of the SCA timing and control. This PLD has connected to it receivers for the 8 trigger signals coming from the trigger system, and drivers for the clock and control signals to the SCAs on the **FEE**. The PLD allows easy reprogramming to adapt to changing requirements.

Power regulators receive raw power from an external power supply and provide regulated power at several levels to a front connector and the back plane for the other 2 boards.

A mezzanine slow controls board will be connected to the PTB via a 64 pin connector. This mezzanine board is currently under development by F. Bieser at LBL. The slow control EPROM will be customized for the readout application. Since slow controls can also be used to dump a whole event (the equivalent of the data from the 8 analog inputs) to the **Readout Electronics**, a transceiver will present this data to the backplane bus in 40-bit chunks. A stored event also can be read out via slow controls through this transceiver over the backplane. A slow instrumentation A/D will be provided for thermistor input to slow controls and the carrier ID will be able to be read if provided.

The tasks of the AMB are to receive the analog data from 8 **Hybrids**, convert the analog samples to digital, provide buffering between the input frequency of the analog samples and the transmission frequency over the Gigalink fiber, and to provide possible storage for the digital data (to be loaded either from the ADCs or from the slow controls interface on the PTB). To provide for the difference in speed of the analog input and the Gigalink transmission frequency, the AMB stores all data in a 40-bit wide fast SRAM which acts as a buffer. The stored data can then be send at full speed to the FOB over the backplane in 40-bit chunks (presented by a 40-bit transceiver). This SRAM is also addressable over the backplane via a 20-bit address buffer. The timing and control of the AMB is done via an Altera PLD. The 8 ADCs of the AMB are read out by the AMB in two banks of 4 ADCs each. Current preference for the choice of these ADCs is the Analog Devices AD875, which can provide 10-bit data at 15 MHz and a precision of 0.4 LSB. However, several types of ADCs (probably 3 different ones) will be provided on the AMB. The parts for the current AMB design populate only about half of the real estate on a 6U VME board. However, we plan to implement the AMB as a full 6U board for possible extension to the full 18 analog channels required for the SVT **Readout Electronics**. It is possible to manufacture the AMB with traces for all 18 channels and only populate 8 of them for the *System Test* .

The FOB contains the necessary parts for reading the digital data from the AMB in 40-bit chunks, convert them to the necessary level to present them to the HP Gigalink Transmitter in 20-bit words, and the fiber-optic transmitter laser diode (either from Finisar or from Methode). It will be necessary to test if the HP Gigalink transmitter can drive two photodiode transmitters, in case this kind of redundancy is desired for the final design. The FOB will provide space for two photodiodes, however, only one will be populated initially. Central timing and control is again achieved with an Altera PLD. The real estate needed for the parts of the FOB could fit on half of a 6U VME board, but for ease of handling a full 6U board will be used.

test plan:

- multiplexing functionality
- readout functionality
- readout speed
- power consumption
- noise

personnel:

coordinator: Bob Minor (LBL), Jo Schambach (UT)

design: Granville Ott (UT), Bob Minor (LBL)
production: Granville Ott (UT), Vendor near Austin
testing: Granville Ott (UT), Jo Schambach (UT), Paul Jensen (UT)

timelines:

Table 6 gives the timelines for the **Readout Electronics** tasks.

Task	Start Date	Completion Date
Readout Electronics design	January 1995	April 1995
Readout Electronics production	April 1995	September 1995
Readout Electronics testing	September 1995	January 1996

Table 6: Timelines for **Readout Electronics** work

3.7 Data Acquisition (DAQ) Receiver Electronics

requirements: A data acquisition (**DAQ**) system to receive digital data from the **Readout Electronics**.

justification: The digitized data from the **Readout Electronics** must be transported to the data acquisition (**DAQ**) electronics where it will be processed.

description of hardware: The DAQ electronics for the *System Test* will consist of a commercial VME processor board by Cyclone Microsystems with an Intel 80960 (i960) processor, and a custom mezzanine board containing the HP Gigalink receiver, 2 Mb of VRAM, and control logic.

description of integration: The mezzanine card is currently being designed and constructed by the DAQ group at BNL as a custom SQUALL module, so that it can be connected and read out by the Cyclone boards i960. The i960 will appear as an intelligent peripheral to the VME system, so that it can be integrated into a VME DAQ system as a data source. A command interface to the Cyclone board is described in the document DAQ temporary receiver card: Command/Response definitions by M. LeVine.

test plan:

personnel:

coordinator: Mike Levine (BNL)

design: Michi Botlo (BNL), Mike Levine (BNL)
production: Brookhaven National Laboratory
testing: Jo Schambach (UT), Granville Ott (UT), Paul Jensen (UT)

timelines:
Table 7 gives the timelines for the **DAQ Receiver Electronics** tasks.

Task	Start Date	Completion Date
Receiver Electronics design	January 1995	April 1995
Receiver Electronics production	April 1995	September 1995
Receiver Electronics testing	September 1995	January 1996

Table 7: Timelines for **DAQ Reciever Electronics** work

3.8 Data Acquisition (DAQ) Processors and Tape Storage

requirements: Data acquisition processor(s) and software for data analysis and storing data on magnetic tape.

justification: A data acquisition system is needed for on-line control, monitoring, taping, and analysis of data.

description of hardware: The **DAQ** hardware will consist of the following:

- 1 VME crate
- 1 MVME167 processor
- 1 Sun LX workstation
- 1 8mm tape drive
- Ethernet connection

description of integration: Software will be written for the *System Test* DAQ system (the Cyclone board and a Motorola VME processor). This software might incorporate some board will not achieve the data throughput rates expected for the final DAQ Receiver boards, which need to receive up to 100 events/sec. This is due to the limited processor power of the Cyclone board (one i960 instead of 18 ASICs and 3 i960s). Therefore the expected data rate during the system test will be more in the order of a few events rather than the full 100 events/sec capability of the **FEE**. However, the higher rate is not required for the *System Test*, so a lower rate is acceptable.

test plan:

personnel:

coordinator: Jo Schambach (UT)

design: Jo Schambach (UT)
building: Jo Schambach (UT), Paul Jensen (UT)
testing: Jo Schambach (UT), Paul Jensen (UT)

timelines:

Table 8 gives the timelines for the **DAQ** tasks.

Task	Start Date	Completion Date
DAQ design	May 1995	August 1995
DAQ building	August 1995	October 1995
DAQ testing	October 1995	December 1995

Table 8: Timelines for **DAQ** work