HLP 3m Message Contents

8/20/2010

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Description	CANScript Command <TargetOp>	HLPS <dir>	Command in Packet ID (Message Header)	Message Length	Payload 0 7654 3210	0	1	2	3	4	5	6	7	Min TDIG code ver	Min TCPU code ver	CAN_HLP3.H symbol
TDC Event Data																
TDC data (need ability to turn on/off)	none		Data (1)	4 or 8		< TDC / TRIGGER Data 1 >				< TDC / TRIGGER Data 2>				11c	1c	C_DATA
Write /Read Sequences (generic)																
Write to Target	**SEND or GSND**		Write (2)	varies	"Address"	Data	additional data depends on length									C_WRITE
"Write Reply" (See Table 1 for status codes)			Write Response (3)	2	Copied from addres	Status										C_WRITE_REPLY
Read from Target	**SEND or GSND**		Read (4)	varies	"Address"											C_READ
Read reply from target			Read Response (5)	varies	Copied from addres	Data result depends on length										C_READ_REPLY
Read reply from Invalid or unimplemented read			Read Response (5)	1	Copied from address											C_READ_REPLY
Alert Sequence (generic)																
Alert/Status			Alert (7)	varies	see section "Alert Conditions"											C_ALERT
1.2.2 Large-Block Write Sequence (generic)																
Block Start	**SEND or GSND**		Write (2)	1 to 8	0001 0000 **0x10**	data to download								11c	1c	C_WS_BLOCKSTART
Block Data	**SEND or GSND**		Write (2)	1 to 8	0010 0000 **0x20**	data to download								11c	1c	C_WS_BLOCKDATA
Block End	**SEND or GSND**		Write (2)	1	0011 0000 **0x30**									11c	1c	C_WS_BLOCKEND
Write Reply w/status, #bytes, Checksum			Write Response (3)	8	0011 0000 **0x30**	Status	bytesL	bytesH	Cksum	Cksum	Cksum	Cksum		11c	1c	
Block Target [tttt] determines target.			Write (2)	1 or more	0100 tttt **0x4tttt**	target address				erase						
Configuration and control for HPTDCs, see below			Write (2)	1	0100 0100 **0x40 thru 0x4B**											C_WS_TARGETHPTDC*, C_WS_TARGETCFG*, C_WS_TARGETCTRL*
MCU program memory;address and erase interpretation depend on target.			Write (2)	6	0100 1100 **0x4C**	target address				erase						C_WS_TARGETMCU
EEPROM#2; Address and erase interpretation depend on target			Write (2)	6	0100 1110 **0x4E**	target address				erase						C_WS_TARGETEEPROM2
2. HPTDC CONTROL, STATUS, and CONFIGURATION																
2.1 Set Control Word to HPTDC															na	
Set Control word to TDC #1, #2, and #3	**W CTRLTDCA**		Write (2)	6	0000 0100 **0x04**	Control Word (40 bits) to all 3 TDCs								11c	na	C_WS_CONTROLTDCS
Set Control word to TDC #1	**W CTRLTDC1**		Write (2)	6	0000 0101 **0x05**	Control Word (40 bits) to TDC #1								11c	na	C_WS_CONTROLTDC1
Set Control word to TDC #2	**W CTRLTDC2**		Write (2)	6	0000 0110 **0x06**	Control Word (40 bits) to TDC #2								11c	na	C_WS_CONTROLTDC2
Set Control word to TDC #3	**W CTRLTDC3**		Write (2)	6	0000 0111 **0x07**	Control Word (40 bits) to TDC #3								11c	na	C_WS_CONTROLTDC3
Set Control word reply			Write Response (3)	8	0011 0000 **0x04 thru 0x07**	Status(i)								11c	na	
2.2 Set Default Control Word to MCU Memory															na	
Block Start	**SEND or GSND**		Write (2)	1 to 8	0001 0000 **0x10**	data to download								11c	1c	C_WS_BLOCKSTART
Block Data	**SEND or GSND**		Write (2)	1 to 8	0010 0000 **0x20**	data to download								11c	1c	C_WS_BLOCKDATA
Block End	**SEND or GSND**		Write (2)	1	0011 0000 **0x30**									11c	1c	C_WS_BLOCKEND
Write Reply w/status, #bytes, Checksum			Write Response (3)	8	0011 0000 **0x30**	Status	bytesL	bytesH	Cksum	Cksum	Cksum	Cksum		11c	1c	
Block Target [tttt] determines target.			Write (2)	1 or more	0100 tttt **0x4tttt**	target address				erase						
Block Target is all 3 HPTDCs control memory	**W BTCTRLMEMA**		Write (2)	1	0100 0100 **0x48**									11c	na	C_WS_TARGETCTRLS
Block Target is HPTDC #1 control memory	**W BTCTRLMEM1**		Write (2)	1	0100 0101 **0x49**									11c	na	C_WS_TARGETCTRL1

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Block Target is HPTDC #2 control memory	**W BTCTRLMEM2**		Write (2)	1	0100 0110	**0x4A**								11c	na	C_WS_TARGETCTRL2
Block Target is HPTDC #3 control memory	**W BTCTRLMEM3**		Write (2)	1	0100 0111	**0x4B**								11c	na	C_WS_TARGETCTRL3
Block Target reply			Write Response (3)	2	0001 00xx	**0x40 thru 0x4B**	status								na	
2.3 Read HPTDC Control Word															na	
Request Report All HPTDC Control word	**R REQCTRLTDCA**		Read (4)	1	0000 0100	**0x00**									na	C_RS_CONTROLTDCS
Request Report HPTDC #1 Control word	**R REQCTRLTDC1**		Read (4)	1	0000 0101	**0x01**								11X	na	C_RS_CONTROLTDC1
Request Control word reply			Read Response (5)	6	0000 0101	**0x01**	Control Word (40 bits) from TDC #1							11X	na	
Request Report HPTDC #2 Control word	**R REQCTRLTDC2**		Read (4)	1	0000 0110	**0x02**								11X	na	C_RS_CONTROLTDC2
Request Control word reply			Read Response (5)	6	0000 0110	**0x02**	Control Word (40 bits) from TDC #2							11X	na	
Request Report HPTDC #3 Control word	**R REQCTRLTDC3**		Read (4)	1	0000 0111	**0x03**								11X	na	C_RS_CONTROLTDC3
Request Control word reply			Read Response (5)	6	0000 0110	**0x03**	Control Word (40 bits) from TDC #3							11X	na	
2.4 Get Status HPTDC															na	
Request Status word from TDC #1	**R STATTDC1**		Read (4)	1	0000 0101	**0x05**									na	C_RS_STATUS1
Request Status word from TDC #2	**R STATTDC2**		Read (4)	1	0000 0110	**0x06**									na	C_RS_STATUS2
Request Status word from TDC #3	**R STATTDC3**		Read (4)	1	0000 0111	**0x07**									na	C_RS_STATUS3
Reply Status word from TDC #1 part 1 of 2			Read Response (5)	8	0000 0101	**0x05**	bits 0 to 55 of status word								na	
Reply Status word from TDC #2 part 1 of 2			Read Response (5)	8	0000 0110	**0x06**	bits 0 to 55 of status word								na	
Reply Status word from TDC #3 part 1 of 2			Read Response (5)	8	0000 0111	**0x07**	bits 0 to 55 of status word								na	
Reply Status word from TDC #1 part 2 of 2			Read Response (5)	2	0000 0101	**0x05**	bits 56 to 63 of status word								na	
Reply Status word from TDC #2 part 2 of 2			Read Response (5)	2	0000 0110	**0x06**	bits 56 to 63 of status word								na	
Reply Status word from TDC #3 part 2 of 2			Read Response (5)	2	0000 0111	**0x07**	bits 56 to 63 of status word								na	
2.5 Configure HPTDC															na	
Block Start	**W BLKSTART**		Write (2)	1 to 8	0001 0000	**0x10**	Optional data to download (0 to 7 bytes)							11c	na	C_WS_BLOCKSTART
Block Data (11 msgs each w/ 7 bytes + 1 msg w/ 4 bytes)	**W BLKDATA**		Write (2)	1 to 8	0010 0000	**0x20**	data to download (0 to 7 bytes)							11c	na	C_WS_BLOCKDATA
Block End	**W BLKEND**		Write (2)	1	0011 0000	**0x30**								11c	na	C_WS_BLOCKEND
Write Reply w/status, #bytes, Checksum			Write Response (3)	8	0011 0000	**0x30**	Status	bytesL	bytesH	Cksum	Cksum	Cksum	Cksum	11c	na	
Block Target [tttt] determines target.			Write (2)	1	0100 tttt	**0x4tttt**								11c	na	see below
Block Target all 3 HPTDCs Configuration	**W BTCFGTDCA**		Write (2)	1	0100 0100	**0x40**								11c	na	C_WS_TARGETHPTDCS
Block Target is HPTDC #1 Configuration	**W BTCFGTDC1**		Write (2)	1	0100 0101	**0x41**								11c	na	C_WS_TARGETHPTDC1
Block Target is HPTDC #2 Configuration	**W BTCFGTDC2**		Write (2)	1	0100 0110	**0x42**								11c	na	C_WS_TARGETHPTDC2
Block Target is HPTDC #3 Configuration	**W BTCFGTDC3**		Write (2)	1	0100 0111	**0x43**								11c	na	C_WS_TARGETHPTDC3
Write Reply w/status			Write Response (3)	2	0011 0000	**0x30**	Status(1)							11c	na	
2.6 Save to HPTDC Configuration Default															na	
Block Start	**W BLKSTART**		Write (2)	1 to 8	0001 0000	**0x10**	Optional data to download (0 to 7 bytes)							11c	na	C_WS_BLOCKSTART
Block Data (11 msgs each w/ 7 bytes + 1 msg w/ 4 bytes)	**W BLKDATA**		Write (2)	1 to 8	0010 0000	**0x20**	data to download (0 to 7 bytes)							11c	na	C_WS_BLOCKDATA
Block End	**W BLKEND**		Write (2)	1	0011 0000	**0x30**								11c	na	C_WS_BLOCKEND
Write Reply w/status, #bytes, Checksum			Write Response (3)	8	0011 0000	**0x30**	Status	bytesL	bytesH	Cksum	Cksum	Cksum	Cksum	11c	na	
Block Target [tttt] determines target.			Write (2)	1 or more	0100 tttt	**0x4tttt**	target address				erase					see below
Block Target is all 3 HPTDCs Configuration memory	**W BTCFGMEMA**		Write (2)	1	0100 0100	**0x44**									na	C_WS_TARGETCFGS
Block Target is HPTDC #1 Configuration memory	**W BTCFGMEM1**		Write (2)	1	0100 0101	**0x45**									na	C_WS_TARGETCFG1

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Block Target is HPTDC #2 Configuration memory	**W BTCFGMEM2**		Write (2)	1	0100 0110	**0x46**									na	C_WS_TARGETCFG2
Block Target is HPTDC #3 Configuration memory	**W BTCFGMEM3**		Write (2)	1	0100 0111	**0x47**									na	C_WS_TARGETCFG3
Write Reply w/status			Write Response (3)	2	0011 0000	**0x30**	Status(1)								na	
2.7 Read HPTDC Configuration															na	
Request Report All HPTDC Configurations	**R REQCFGTDCA**		Read (4)	1	0100 0100	**0x40**								11X	na	C_RS_CONFIGTDCS
Request replies will be 12 replies per HPTDC. 36 replies total. Payload[0] will indicate TDC 1, 2, or 3.			Read Response (5)													
Request HPTDC Configuration reply #1 of 12			Read Response (5)	8	0100 01xx	**0x4?**	bits 0..55 of Configuration memory							11X	na	
Request configuration reply # 2 thru 11 of 12			Read Response (5)	8	0100 01xx	**0x4?**	successive bits of configuration memory							11X	na	
Request configuration reply #12 of 12			Read Response (5)	5	0100 01xx	**0x4?**	bits 615..646 of configuration memory							11X	na	
Request Report HPTDC #1 Configuration	**R REQCFGTDC1**		Read (4)	1	0100 0101	**0x41**								11X	na	C_RS_CONFIGTDC1
Request Report HPTDC #2 Configuration	**R REQCFGTDC2**		Read (4)	1	0100 0110	**0x42**								11X	na	C_RS_CONFIGTDC2
Request Report HPTDC #3 Configuration	**R REQCFGTDC3**		Read (4)	1	0100 0111	**0x43**								11X	na	C_RS_CONFIGTDC3
Request HPTDC Configuration reply #1			Read Response (5)	8	0100 01xx	**0x4?**	bits 0..55 of Configuration memory							11X	na	
Request configuration reply # 2 thru 11 of 12			Read Response (5)	8	0100 01xx	**0x4?**	successive bits of configuration memory							11X	na	
Request configuration reply #12 of 12			Read Response (5)	5	0100 01xx	**0x4?**	bits 615..646 of configuration memory							11X	na	
2.8 Issue HPTDC Reset Sequence															na	
Issue Reset sequence to all 3 HPTDCs	**W RESETTDCA**		Write (2)	1	1001 0000	**0x90**									na	C_WS_RSTSEQHPTDCS
Issue Reset sequence to HPTDC #1	**W RESETTDC1**		Write (2)	1	1001 0001	**0x91**									na	C_WS_RSTSEQHPTDC1
Issue Reset sequence to HPTDC #2	**W RESETTDC2**		Write (2)	1	1001 0010	**0x92**									na	C_WS_RSTSEQHPTDC2
Issue Reset sequence to HPTDC #3	**W RESETTDC3**		Write (2)	1	1001 0011	**0x93**									na	C_WS_RSTSEQHPTDC3
Issue Reset sequence reply			Write Response (3)	2	1001 00xx	**0x90 thru 0x93**	status								na	

3. CONFIGURE / CONFIRM BOARD OPTIONS AND STATUS																
3.1 Board Status																
3.1.1 Request Status word from TDIG Board	**R BRDSTATUS**		Read (4)	1	1011 0000	**0xB0**								11U	na	C_RS_STATUSB
Reply Status word from TDIG BOARD (MCU)			Read Response (5)	8	1011 0000	**0xB0**	Tmp L	Tmp H	ECSR	AD 1L	AD 1H	AD 2L	AD2H	11U	na	
3.1.2 Request Status word from TCPU Board	**R BRDSTATUS**		Read (4)	1	1011 0000	**0xB0**								na	1f	C_RS_STATUSB
Reply Status word from TCPU BOARD (MCU)			Read Response (5)	8	1011 0000	**0xB0**	Tmp L	Tmp H	ECSR	0	0	0	0	na	1f	
3.1.3 Request Firmware Identifiers	**R FIRMWAREID**		Read (4)	1	1011 0001	**0xB1**								11d	1g	C_RS_FIRMWID
Firmware Identifiers reply			Read Response (5)	4	1011 0001	**0xB1**	MCU.L	MCU.H	FPGA					11d	1g	
3.1.4 Request Board Serial Number	**R HDWSERNBR**		Read (4)	1	1011 0010	**0xB2**								11c	1f	C_RS_SERNBR
Board Serial Number Reply			Read Response (5)	8	1011 0010	**0xB2**	SN	SN	SN	SN	SN	SN	SN	11c	1f	
3.1.5 Request Jumper/Switch Inputs	**R JMPRSW**		Read (4)	1	1011 0011	**0xB3**								11c	1f	C_RS_JSW
Jumper/Switch Inputs Reply TCPU Table 4			Read Response (5)	2	1011 0011	**0xB3**	JSW							na	1f	
Jumper/Switch Inputs Reply TDIG Table 5			Read Response (5)	2	1011 0011	**0xB3**	JSW							11c	na	
3.1.6 Request ECSR Value from U36 TDIG	**R ECSR**		Read (4)	1	1011 0100	**0xB4**								11c	1f	C_RS_ECSR
ECSR Value Reply TCPU Table 2			Read Response (5)	2	1011 0100	**0xB4**	ECSR							na	1f	

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3.1.7 Request ECSR Value from U36 TDIG	**R ECSR**	Read (4)	1	1011 0100	**0xB4**								11c	1f	C_RS_MCUSTATUS
ECSR Value Reply TDIG Table 3		Read Response (5)	2	1011 0100	**0xB4**	ECSR							11c		
3.1.8 Request MCU Status	**R MCUSTATUS**	Read (4)	1	1011 0101	**0xB5**										C_RS_DIAGNOSTIC
MCU Status Reply		Read Response (5)	5	1011 0101	**0xB5**	Reset Vector Contents (debug)								2F	
MCU Status Reply		Read Response (5)	3	1011 0101	**0xB5**	MCU CLOCK		<tbd>							
3.2 Board Control															
3.2.1 Write Threshhold DAC	**W THRESHHOLD**	Write (2)	3	0000 1000	**0x08**	Thr L	Thr H						11c	na	C_WS_THRESHHOLD
Write Threshhold DAC reply		Write Response (3)	2	0000 1000	**0x08**	status							11c	na	
3.2.2 Request Threshhold Setting	**R THRESHHOLD**	Read (4)	1	0000 1000	**0x08**								11U	na	
Request Threshhold Setting Reply		Read Response (5)	3	0000 1000	**0x08**	Thr L	Thr H						11U	na	
Temperature Read and Temperature Alert control														na	
3.2.3 Request Board Temperature(s)	**R TEMPERATURE**	Read (4)	1	0000 1001	**0x09**								11c	1f	C_RS_TEMPBRD
3.2.3.1Request Temperature Reply (TDIG/TINO)		Read Response (5)	7	0000 1001	**0x09**	Tmp L	Tmp H	Tino1L	TinoH	Tino2L	Tino2H		11U		
3.2.3.2 Request Temperature Reply (TCPU)		Read Response (5)	3	0000 1001	**0x09**	Tmp L	Tmp H							1f	
3.2.4.1 Write Temperature Alert Settings (TDIG)	**W TEMPALERT**	Write (2)	7	0000 1001	**0x09**	Tmp L	Tmp H	Tino1L	TinoH	Tino2L	Tino2H		11V	na	C_WS_TEMPALERTS
						Only upper 9 bits of Tmp* are used!									
Write Temperature alert Settings Reply (TDIG)		Write Response (3)	2	0000 1000	**0x09**	status							11V	na	
3.2.4.2 Write Temperature Alert Setting (TCPU)	**W TEMPALERT**	Write (2)	3	0000 1001	**0x09**	Tmp L	Tmp H						na	2G	C_WS_TEMPALERTS
						Only upper 9 bits of Tmp* are used!								2G	
Write Temperature Alert Settings Reply (TCPU)		Write Response (3)	2	0000 1000	**0x09**	status							na	2G	
		IS THIS RIGHT?													
3.2.5 Board Clock Options															
3.2.5 Board Clock Source	**W CLOCKS**	Write (2)	3	0000 1101	**0x0D**	req'd	req'd						11r		C_WS_OSCSRCSEL
Local/Remote Oscillator Select request (req'd must match) req'd=0xFF use jumper; req'd=0x00 use Board; req'd=0x08 use Tray; req'd=0x01 MCU Uses internal FRC w/PLL independent of board/tray		Write (2)	3	0000 1101	**0x0D**	req'd	req'd						11r		
3.2.6 Request clock status	**R CLOCKS**	Read (4)	1	0000 1010	**0x0D**								11r		C_RS_CLKSTATUS
Clock Status reply (req'd = code as above)		Read Response (5)	5	0000 1010	**0x0D**	OSCCON		failed	req'd				11r	2F	
Board Miscellaneous and reserved															
FPGA Configure / Reset															
Reconfigure FPGA from EEPROM #1 (default)		see FPGA / EEPROM below											11c	1f	C_WS_RECONFIGEE1
Reconfigure FPGA from EEPROM #2		see FPGA / EEPROM below											11c	1c	C_WS_RECONFIGEE2
MCU Configure / Reset															

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Restart MCU, Code Image #1			see MCU below													C_WS_MCURESET
Restart MCU, Code Image #2 (download)			see MCU below													C_WS_MCURESTARTA
Board Diagnostics and Testing																
3.2.7 TINO Test Pulse																
3.2.7.1 Toggle TINO_TEST_MCU line once.	**W TINOTGL1**		Write (2)	1	0000 1111	**0x0F**								11U	na	C_WS_TOGGLETINO
3.2.7.2 Toggle TINO_TEST_MCU line "CNT" times.	**W TINOTGLN**		Write (2)	3	0000 1111	**0x0F**	Cnt L	Cnt H						11U	na	C_WS_TOGGLETINO
Toggle TINO_TEST_MCU line Reply			Write Response (3)	2	0000 1111	**0x0F**	status							11U	na	
3.2.8 Reserved for Diagnostics and Testing																
Diagnostic write	**W DIAGNOSTIC**		Write (2)	1 to 8	1111 1111	**0xFF**	<as needed for diagnostic function>									C_WS_DIAGNOSTIC
Diagnostic write reply			Write Response (3)	1 to 8	1111 1111	**0xFF**	<as needed for diagnostic function>									
Diagnostic read	**R DIAGNOSTIC**		Read (4)	1 to 8	1111 1111	**0xFF**	<as needed for diagnostic function>									C_RS_DIAGNOSTIC
Diagnostic read reply			Read Response (5)	1 to 8	1111 1111	**0xFF**	<as needed for diagnostic function>									
3.2.9 Write LED pattern	**W LED**		Write (2)	2	0000 1010	**0x0A**	LED							11c	1f	C_WS_LED
Request LED pattern	**R LED**		Read (4)	1	0000 1010	**0x0A**										C_RS_LED
LED pattern reply			Read Response (5)	2	0000 1010	**0x0A**	LED									
HPTDC Power On/Off (PWR must match)	**W POWER**		Write (2)	3	0000 1011	**0x0B**	PWR	PWR							na	C_WS_TDCPOWER
Silent mode (no MCU Readout)			Write (2)	2			0000 0000							na	na	
Serial Data Readout via PLD FIFO			Write (2)	2			0x01							na	na	
JTAG readout			Write (2)	2			0000 0010							na	na	

4. FPGA / EEPROM CONTROL AND CONFIGURATION																
4.1 FPGA_WRITE_to_register (PLD_WRITE_REG)																
Write to 1, 2, or 3 FPGA Registers	**W FPGAREG**		Write (2)	3, 5, or 7	0000 1110	**0x0E**	adr	data	[adr1	data1]	[adr2	data2]		11c	1c	C_WS_FPGAREG
Write to 1, 2, or 3 FPGA Registers response			Write Response (3)	2	0000 1110	**0x0E**	status							11c	1c	
4.2 FPGA_READ_from_register (PLD_READ_REG)																
Read from 1, 2, or 3 FPGA Registers	**R FPGAREG**		Read (4)	2, 3, or 4	0000 1110	**0x0E**	adr	[adr1	adr2]					11c	1c	C_RS_FPGAREG
Read from 1, 2, or 3 FPGA Registers Reply			Read Response (5)	3, 5, or 7	0000 1110	**0x0E**	adr	data	[adr1	data1]	[adr2	data2]		11c	1c	
4.3 FPGA_RECONFIGURE from EEPROM #1																
Reconfigure FPGA from EEPROM #1 (default)	**W RECONF1**		Write (2)	5	1000 1001	**0x89**	0x69	0x96	0xA5	0x5A				11c	1c	C_WS_RECONFIGEE1
Write Reply w/status, ID from Reg 7			Write Response (3)	3	1000 1001	**0x89**	Status	ID						11c	1c	
4.4 FPGA_RECONFIGURE from EEPROM #2																
Reconfigure FPGA from EEPROM #2 (dnload)	**W RECONF2**		Write (2)	5	1000 1010	**0x8A**	0x69	0x96	0xA5	0x5A				11c	1c	C_WS_RECONFIGEE2
Write Reply w/status, ID from Reg 7			Write Response (3)	3	1000 10xx	**0x8A**	Status	ID						11c	1c	

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4.5 FPGA_RESET (PLD_RESET)															
PLD hardware Reset pulse	**W FPGARESET**	Write (2)	5	0000 1100	**0x0C**	0x69	0x96	0xa5	0x5a				11c	1c	C_WS_FPGARESET
PLD hardware Reset pulse reply		Write Response (3)	2	0000 1100	**0x0C**	status							11c	1c	
4.6 Download EEPROM #2 (FPGA) Code															
4.6.1 Block Start	**W BLKSTART**	Write (2)	1 to 8	0001 0000	**0x10**	Optional data to download (0 to 7 bytes)							11c	1c	C_WS_BLOCKSTART
4.6.2 Block Data (36 msgs each w/ 7 bytes + 1 msg w/ 4 bytes)	**W BLKDATA**	Write (2)	1 to 8	0010 0000	**0x20**	data to download (0 to 7 bytes)							11c	1c	C_WS_BLOCKDATA
4.6.3 Block End	**W BLKEND**	Write (2)	1	0011 0000	**0x30**								11c	1c	C_WS_BLOCKEND
Write Reply w/status, #bytes, Checksum		Write Response (3)	8	0011 0000	**0x30**	Status	bytesL	bytesH	Cksum	Cksum	Cksum	Cksum	11c	1c	
4.6.4 Block Target is EEPROM #2 (w/o or w/erase)	**W BTEEPROM2**	Write (2)	6	0100 1110	**0x4E**	<eeprom sector address>				erase			11c	1c	C_WS_TARGETEEPROM2
Block Target reply		Write Response (3)	2	0100 1110	**0x4D**	Status							11c	1c	
4.6.5 Set FPGA CONFIG to 0		Write (2)	1	0001 0001	**0x11**										C_WS_FPGA_CONF0
4.6.5 Set FPGA CONFIG to 1		Write (2)	1	0001 0010	**0x12**										C_WS_FPGA_CONF1
4.7.1 and 4.7.2 Read EEPROM #2 Contents															
Read 7 bytes from EEPROM #2 address	**R EEPROM2**	Read (4)	5	0100 1110	**0x4E**	<eeprom sector address>							11T	2F	C_RS_EEPROM2
7 bytes Data read from EEPROM #2 address		Read Reply (5)	8	0100 1110	**0x4E**	memory contents							11T	2F	
Checksum EEPROM #2 Contents															
4.8 Read and checksum EEPROM #2, sector=256 bytes	**R EEPROM2CKSUM**	Read (4)	8	0100 1111	**0x4F**	<eeprom start address>				<# sectors to read>			11T	2F	C_RS_EEP2CKSUM
Checksum of bytes from EEPROM #2		Read Reply (5)	5	0100 1111	**0x4F**	<eeprom checksum>							11T	2F	
5. MCU CONTROL AND CONFIGURATION															
5.1 Start MCU Code Image #1 (power-up image)															
MCU Reset (POR equivalent) First Image	**W MCUSTART1**	Write (2)	5	1000 1111	**0x8F**	0x69	0x96	0xa5	0x5a				11d	1h	C_WS_MCURESET
MCU Reset acknowledge (followed by ALERT)		Write Response (3)	2	1000 1111	**0x8F**	Status							11d	1h	
5.2 Start MCU Code Image #2 (downloaded image)															
MCU Start Second Image	**W MCUSTART2**	Write (2)	5	1000 1101	**0x8D**	0x69	0x96	0xa5	0x5a				11d	1h	C_WS_MCURESTARTA
MCU Start Second Image reply		Write Response (3)	2	1000 1101	**0x8D**	status							11d	1h	
Automagic Second Image Startup															
Write to Magic Number Location		Write (2)	3	1000 1111	**0x4F**										C_WS_MAGICNUMWR
Write to Magic Number Location Reply		Write Response (3)	2	1000 1111	**0x4F**	Status									
5.3 Download MCU Code															
5.3.1 Block Start	**W BLKSTART**	Write (2)	1 to 8	0001 0000	**0x10**	Optional data to download (0 to 7 bytes)							11c	1c	C_WS_BLOCKSTART
5.3.2 Block Data	**W BLKDATA**	Write (2)	1 to 8	0010 0000	**0x20**	Data to download (0 to 7 bytes)							11c	1c	C_WS_BLOCKDATA
5.3.3 Block End	**W BLKEND**	Write (2)	1	0011 0000	**0x30**								11c	1c	C_WS_BLOCKEND
Write Reply w/status, #bytes, Checksum		Write Response (3)	8	0011 0000	**0x30**	Status	bytesL	bytesH	Cksum	Cksum	Cksum	Cksum	11c	1c	
5.3.4 Block Target is MCU address	**W BTMCUMEM**	Write (2)	6	0100 1100	**0x4C**	address				erase			11d	1h	C_WS_TARGETMCU
Block Target is MCU reply		Write Response (3)		0100 1100	**0x4C**	Status							11d	1h	
5.4 Read MCU Memory															
5.4.1 Read from MCU address (1 location)	**R MCUMEM**	Read (4)	5	0100 1100	**0x4C**	memory address							11d	1h	C_RS_MCUMEM
Read from MCU address reply		Read Reply (5)	5	0100 1100	**0x4C**	memory contents							11d	1h	

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5.4.3 Bad Address for memory read			Read Reply (5)	1	0100 1100	**0x4C**								11U	2F	
5.5 Checksum MCU Memory																
Checksum MCU memory range	**R MCUCKSUM**		Read (4)	8	0100 1100	**0x4D**	memory address - start				Address Count			11U	2F	C_RS_MCUCKSUM
MCU checksum reply			Read Reply (5)	6	0100 1100	**0x4D**	memory checksum							11U	2F	
6. Data Transmission																
Disable Data Transmission via CANBus	**W DATAOFF**		Write (2)	2	1101 0000	**0xD0**	0xD0									<tbd>
Disable Data Transmission reply			Write Response (3)	2	1101 0000	**0xD0**	<TBD>									
Enable Data Transmission via CANBus	**W DATAON**		Write (2)	2	1101 0001	**0xD1**	0xD1									<tbd>
Enable Data Transmission via CANBus			Write (2)	2	1101 0001	**0xD1**	0xD1									
7. ALERT CONDITIONS																
MCU Started Up	**SEND or GSND**		Alert (7)	4	1111 1111	**0xFF**	0x0	0x0	0x0					11d	1f	C_ALERT_ONLINE
TDIG Clock Fail	**SEND or GSND**		Alert (7)	1	1111 1100	**0xFC**								11R		C_ALERT_CLOCKFAIL_CODE
TCPU CAN1 Error / Overflow	**SEND or GSND**		Alert (7)	2	1111 1100	**0xC1**	code							11W	2H	C_ALERT_ERRCAN1_CODE
TCPU CAN2 Error / Overflow	**SEND or GSND**		Alert (7)	2	1111 1100	**0xC2**	code							11W	2H	C_ALERT_ERRCAN2_CODE
FPGA CRC Error Detected	**SEND or GSND**		Alert (7)	1	0000 0100	**0x04**								11J	2F	C_ALERT_CKSUM_CODE
TDC Power Error Detected	**SEND or GSND**		Alert (7)	1	0001 0000	**0x10**									na	<tbd>
HPTDC Configuration Mismatch	**SEND or GSND**		Alert (7)	6	0001 0001	**0x11**	TDC#	IndexL	IndexH	Exp'd	Got				na	<tbd>
MCU / TINO Heat Alert(s) Detected (Table 6)	**SEND or GSND**		Alert (7)	2	0000 1001	**0x09**	Mask							11V		C_ALERT_OVERTEMP_CODE
TABLE 1: Status codes (Payload[1])																
OK / Success					depends on		0									C_STATUS_OK
Invalid / Not Implemented					command		1									C_STATUS_INVALID
Block Data/End/Target w/o Block Start							2									C_STATUS_NOSTART
Block Buffer Overrun							3									C_STATUS_OVERRUN
Block Target Unknown							4									C_STATUS_NOTARGET
Checksum Error							5							na	na	C_STATUS_CKSUMERR
Block Target Length Incorrect							6									C_STATUS_LTHERR
Error during HPTDC Reconfiguration							7								na	C_STATUS_BADCFG
Error during EEPROM#2 Write							8									C_STATUS_BADEE2
Timeout during reconfiguration from EEPROM2, FPGA reloaded from EEPROM1.							9									C_STATUS_TMOFPGA
Invalid address during MCU block target							A							11U	2F	C_STATUS_BADADDRS
TABLE 2: Extended CSR (ECSR) BITS for TCPU													Bit			**TCPU-C_Board.H**
PLD_CONFIG DONE (usually 1)			appear in response to										0	na		ECSR_PLD_CONFIG_DONE
PLD_INIT_DONE (usually 1)			"Read Board Status" and										1	na		ECSR_PLD_INIT_DONE
PLD_CRC_ERROR (usually 0)			"Read ECSR"										2	na		ECSR_PLD_CRC_ERROR
PLD_nSTATUS (usually 1)													3	na		ECSR_PLD_NSTATUS
SW1 Pushbutton (1=pressed)													4	na		BUTTON
JU2 Jumper 5-6 (1=jumper installed)													5	na		JUMPER_5_6
JU2 Jumper 3-4 (1=jumper installed)													6	na		JUMPER_3_4
JU2 Jumper 1-2 (1=jumper installed)													7	na		JUMPER_1_2
TABLE 3: Extended CSR (ECSR) BITS for TDIG													Bit			**TDIG-F_Board.H**
PLD_CONFIG DONE (usually 1)			appear in response to										0		na	ECSR_PLD_CONFIG_DONE

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PLD_INIT_DONE (usually 1)			"Read Board Status" and										1		na	ECSR_PLD_INIT_DONE
PLD_CRC_ERROR (usually 0)			"Read ECSR"										2		na	ECSR_PLD_CRC_ERROR
PLD_nSTATUS (usually 1)													3		na	ECSR_PLD_NSTATUS
TDC_POWER_ERROR_B (normally 1)													4		na	ECSR_TDC_POWER_ERROR_B
ENABLE_TDC_POWER (output) (normally 1)													5		na	ECSR_TDC_POWER
TINO_TEST_MCU (output) (normally 0)													6		na	ECSR_TINO_TEST_MCU
SPARE_PLD (usually 1)													7		na	ECSR_SPARE_PLD

TABLE 4: SWITCH BITS for TCPU													Bit			TCPU-C_Board.H
SW4 w1 (board position 2^0)			appear in response to										0	na		Value accessed using:
SW4 w2 (board position 2^1)			"Read Jumper/Switch Settings"										1	na		BOARDSW4_MASK
SW4 w4 (board position 2^2)			Switches are BCD decimal.										2	na		
SW4 w8 (board position 2^3)			Actual board-position is masked to the range [0..31]										3	na		
SW5 w10 (board position 2^0 * 10)													4	na		Value accessed using:
SW5 w20 (board position 2^1 * 10)													5	na		BOARDSW5_MASK
SW5 w40 (board position 2^2 * 10)													6	na		
SW5 w80 (board position 2^3 * 10)													7	na		

TABLE 5: SWITCH BITS for TDIG													Bit			TDIG-F_Board.H
SW1 pushbutton (1=pressed)			appear in response to										0		na	BUTTON
SW4 w4 (board position 2^2)			"Read Jumper/Switch Settings"										1		na	Value accessed using:
SW4 w2 (board position 2^1)													2		na	BOARDSW4_MASK and
SW4 w1 (board position 2^0)			Actual board-position is masked to the range [0..7]										3		na	BOARDSW4_SHIFT
JU2 7-8 (1=jumper installed)													4		na	JUMPER_7_8
JU2 5-6 (1=jumper installed)													5		na	JUMPER_5_6
JU2 3-4 (1=jumper installed)													6		na	JUMPER_3_4
JU2 1-2 (1=jumper installed)													7		na	JUMPER_1_2

TABLE 6: MASK BITS for OVERTEMPERATURE ALERT (Payload[1])													Bit			CAN_HLP3.H symbol
MCU is Over limit			Appear in byte 1 of Alert Message										0	11V	na	ALERT_MASK_MCU
TINO1 Overtemperature			over_limit condition occurs										1	11V	na	ALERT_MASK_TINO1
TINO2 Overtemperature													2	11V	na	ALERT_MASK_TINO2
															na	
															na	
															na	
															na	
															na	

TABLE 7: Message Type Code Summary (by value)															CAN_HLP3.H symbol
Description		Direction			Payload [0]										
Read Last Control Word from all 3 TDCs		Read			0x00								11X	na	C_RS_CONTROLTDCS
Read Last Control Word from TDC #1		Read			0x01								11X	na	C_RS_CONTROLTDC1
Read Last Control Word from TDC #2		Read			0x02								11X	na	C_RS_CONTROLTDC2
Read Last Control Word from TDC #3		Read			0x03								11X	na	C_RS_CONTROLTDC3
Write Control Word to all 3 TDCs		Write			0x04									na	C_WS_CONTROLTDCS

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Write Control Word to TDC #1			Write			**0x05**									na	C_WS_CONTROLTDC1
Read Status Word from TDC #1			Read			**0x05**									na	C_RS_STATUS1
Write Control Word to TDC #2			Write			**0x06**									na	C_WS_CONTROLTDC2
Read Status Word from TDC #2			Read			**0x06**									na	C_RS_STATUS2
Write Control Word to TDC #3			Write			**0x07**									na	C_WS_CONTROLTDC3
Read Status Word from TDC #3			Read			**0x07**									na	C_RS_STATUS3
Threshhold Set			Write			**0x08**									na	C_WS_THRESHHOLD
Threshhold Read			Read			**0x08**									na	C_RS_THRESHHOLD
Temperature Alert Set			Write			**0x09**										C_WS_TEMPALERTS
Board Temperature Read			Read			**0x09**										C_RS_TEMPBRD
LED Pattern Set			Write			**0x0A**										C_WS_LED
TDC Power			Write			**0x0B**									na	C_WS_TDCPOWER
FPGA Reset			Write			**0x0C**										C_WS_FPGARESET
Oscillator Source			Write			**0x0D**										C_WS_OSCSRCSEL
FPGA Write Register			Write			**0x0E**										C_WS_FPGAREG
FPGA Read Register			Read			**0x0E**										C_RS_FPGAREG
Generate TINO Test Pulse(s)			Write			**0x0F**									na	C_WS_TOGGLETINO
Block Transfer Start			Write			**0x10**										C_WS_BLOCKSTART
set FPGA CONFIG to 0			Write			0x11										C_WS_FPGA_CONF0
set FPGA CONFIG to 1			Write			0x12										C_WS_FPGA_CONF1
Block Transfer Data			Write			**0x20**										C_WS_BLOCKDATA
Block Transfer End			Write			**0x30**										C_WS_BLOCKEND
Block Data Target all 3 HPTDC			Write			**0x40**									na	C_WS_TARGETHPTDCS
Read All HPTDCs configuration blocks			Read			**0x40**								11X	na	C_RS_CONFIGTDCS
Block Data Target HPTDC #1			Write			**0x41**									na	C_WS_TARGETHPTDC1
Read HPTDC#1 configuration block			Read			**0x41**								11X	na	C_RS_CONFIGTDC1
Block Data Target HPTDC #2			Write			**0x42**									na	C_WS_TARGETHPTDC2
Read HPTDC#2 configuration block			Read			**0x42**								11X	na	C_RS_CONFIGTDC2
Block Data Target HPTDC #3			Write			**0x43**									na	C_WS_TARGETHPTDC3
Read HPTDC#3 configuration block			Read			**0x43**								11X	na	C_RS_CONFIGTDC3
Block Data Target all 3 HPTDC Config. Flash			Write			**0x44**									na	C_WS_TARGETCFGS
Block Data Target HPTDC #1 Config. Flash			Write			**0x45**									na	C_WS_TARGETCFG1
Block Data Target HPTDC #2 Config. Flash			Write			**0x46**									na	C_WS_TARGETCFG2
Block Data Target HPTDC #3 Config. Flash			Write			**0x47**									na	C_WS_TARGETCFG3
Block Data Target all 3 Control Flash			Write			**0x48**									na	C_WS_TARGETCTRLS
Block Data Target HPTDC #1 Control Flash			Write			**0x49**									na	C_WS_TARGETCTRL1
Block Data Target HPTDC #2 Control Flash			Write			**0x4A**									na	C_WS_TARGETCTRL2
Block Data Target HPTDC #3 Control Flash			Write			**0x4B**									na	C_WS_TARGETCTRL3
Block Data Target MCU Memory			Write			**0x4C**										C_WS_TARGETMCU
Read MCU Memory			Read			**0x4C**										C_RS_MCUMEM
Checksum MCU Memory			Read			**0x4D**										C_RS_MCUCKSUM
Block Data Target EEPROM #2			Write			**0x4E**										C_WS_TARGETEEPROM2
Read EEPROM#2 Contents			Read			**0x4E**								11T		C_RS_EEPROM2
Write Magic Number			Write			**0x4F**										C_WS_MAGICNUMWR
Checksum EEPROM #2			Read			**0x4F**										C_RS_EEP2CKSUM
Not Implemented Block Checksum						**0x50**								na	na	C_WS_BLOCKCKSUM
Execute script buffer			Write			0x60								na	2V	C_WS_EXESCRIPT
Load a section of a script entry			Write			0x61								na	2V	C_WS_LDSCRIPTE
Write script entry to PM and RAM			Write			0x62								na	2V	C_WS_WRSCRIPTE
Reconfigure FPGA from image #1			Write			**0x89**										C_WS_RECONFIGEE1
Reconfigure FPGA from image #2			Write			**0x8A**										C_WS_RECONFIGEE2
MCU Start Second Image			Write			**0x8D**										C_WS_MCURESTARTA
MCU (Re)Start First Image			Write			**0x8F**										C_WS_MCURESET
Reset Sequence all 3 HPTDCs			Write			**0x90**									na	C_WS_RSTSEQHPTDCS

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Reset Sequence HPTDC #1			Write			**0x91**									na	C_WS_RSTSEQHPTDC1
Reset Sequence HPTDC #2			Write			**0x92**									na	C_WS_RSTSEQHPTDC2
Reset Sequence HPTDC #3			Write			**0x93**									na	C_WS_RSTSEQHPTDC3
Switch Sending Alarm messages			Write			**0xA0**								na		C_WS_SEND_ALARM
Write Configuration Register			Write			0xA1								12B	na	C_WS_CONF_REG
Request Board Status			Read			**0xB0**										C_RS_STATUSB
Request Firmware Identifiers			Read			**0xB1**										C_RS_FIRMWID
Request Board HDW Serial Number			Read			**0xB2**										C_RS_SERNBR
Request Jumper/Switch settings			Read			**0xB3**										C_RS_JSW
Request Extended CSR			Read			**0xB4**										C_RS_ECSR
Request Clock Status			Read			**0xB5**										C_RS_MCUSTATUS
Disable Data via CANBus			Write			**0xD0**								na	na	<tbd>
Enable Data via CANBus			Write			**0xD1**								na	na	<tbd>
"Extended" message						**0xEx**										
Reserved for Diagnostic Function			W/R			**0xFF**										C_RS_DIAGNOSTIC

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Description			**Alert Codes**			**Payload [0]**										
FPGA CRC Error alert						**0x04**										
MCU / TINO Heat Alert(s) Detected alert						**0x09**										
TDC Power Error Detected alert						**0x10**										
HPTDC Configuration Mismatch alert						**0x11**										
CANBus #1 Overflow / Error alert						**0xC1**										
CANBus #2 Overflow / Error alert						**0xC2**										
Clock Fail alert						**0xFC**										
Startup alert						**0xFF**										

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TDIG PLD Registers	Bit	Description
0x0	0	
	1	TDCs first in Readout Chain
	6	TDC event reset
0x1	0	JTAG mode: 01=TDC1, 10=TDC2, 11=TDC3
	1	JTAG mode (MSb)
	2	JTAG Select: 1=MCU, 0=JTAG header
0x2	0	TDC reset
0x3	0	TDC1 Error Bit
	1	TDC2 Error Bit
	2	TDC3 Error Bit
0xC	0	Board Position (bit0)
	1	Board Position (bit1)
	2	Board Position (bit2)
	3:0	Multiplicity gate width

TCPU PLD Registers	Bit	Description
0x1	0	state machine reset
	1	FIFO clear
0x2	0	readout enable
	1	test pulse (0) or Serdes (1) trigger
	2	CANbus message off (1)
	3	Serdes sync (1)
0x3	0	Serdes Lock_n (ro)
	1	Serdes ready (ro)
0x8	3:0	DSMI Multiplicity clock delay
	7:4	Tray Multiplicity clock delay
0x9	7	Multiplicity (0) or Ramp (1) data
0xE	0	test pulser frequency (bit 0)
	1	test pulser frequency (bit 1)
	2	test pulser frequency (bit 2)
	3	test pulse: J9 (0) or internal (1)
	4	bunch reset (level)
	7	TDC readout through FPGA (1) or Aux path (0)