HLP Messages for THUB

Command in Packet ID (Code)	Message Length	Payload 0 7654 3210	0	1	2	3	4	5	6	7	Description
Trigger Data											
Data(1)	4	<Trigger Data Word>									Trigger Data (4 bytes) from TCD
Write Commands											
Write (2)	2	0000 1010	**0x0A**	<1,0>							Readout Mode: 0 = quiet, 1 = send trigger data
Write (2)	2	0000 1011	**0x0B**	Delay							Test messages with delay; off when delay = 0
Write (2)	2	0000 1100	**0x0C**	<1,0>							Alert Fiber message: 0 = send, 1 = quiet
Write (2)	1	0000 1101	**0x0D**								Reconfigure all FPGAs
Write (2)	2 or 4	1xxx xxxx	**0xXX**	data	[addr2]	[data2]					Write PLD register (1 or 2 addresses and bytes). 0x80 < addr < 0xff
Write (2)	2	0010 0000	**0x20**	num							Start FPGA [num] program. 1-8: Serdes, 0: Master
Write (2)	4	0010 0001	**0x21**	addrL	addrM	addrH					3 byte FPGA EEPROM address
Write (2)	2 to 8	0010 0010	**0x22**	data0	[data1]	[data2]	[data3]	[data4]	[data5]	[data6]	Write 1-7 bytes FPGA EEPROM Data
Write (2)	2 to 8	0010 0011	**0x23**	data0	[data1]	[data2]	[data3]	[data4]	[data5]	[data6]	Write 1-7 bytes FPGA EEPROM Data, program page
Write (2)	1	0010 0100	**0x24**								FPGA EEPROM program end
Write (2)	2 to 8	0010 0101	**0x25**	data0	[data1]	[data2]	[data3]	[data4]	[data5]	[data6]	Write 1-7 bytes MCU Data, program 64byte page
Write (2)	5	0010 0110	**0x26**	addrL	addrH	data	Reset				Write "data" to MCU EEPROM addr <addrH addrL>. If Reset == 0xA5, reset MCU If address = 0xffff, data = 0x0: upper, data = 0xff: lower
Write Response (3)	2	Subcommand		Status(1)							Write Reply
Read Commands											
Read (4)	1	0000 0001	**0x01**								Read MCU Firmware ID
Read (4)	2	0000 0010	**0x02**	<0-8>							Read FPGA Firmware ID. 1-8: Serdes, 0: Master
Read (4)	2	0000 0011	**0x03**	<1,2>							Read Temperature. 1: U131, 2: U132
Read (4)	3	0000 0100	**0x04**	0xX	0xY						Read Voltage. X: 2=U122, 3=U123, 4=U124. Y: ADC_MUX register value
Read (4)	1	0000 0101	**0x05**								Read CRC_Error bits; Byte0[7..0] = [H..A], Byte1[0] = [M]
Read(4)	7	0000 0110	**0x06**	startL	startH	startU	endL	endH	endU		Calculate checksum between "start" and "end"
Read (4)	2	0010 0111	**0x27**	<0..8>							Read PLD EEPROM SiID. 1-8: Serdes, 0: Master
Read (4)	1	1xxx xxxx	**0xXX**								Read PLD Register. 0x80 < addr < 0xff
Alarm Messages											
Alert (7)	4	1111 1111	**0xFF**	0x55	0x0	0x0					Fiber received FECTRL with parameter = 0xabc0
Alert (7)	4	1111 1111	**0xFF**	0xFF	0xFF	0xFF					FPGAs didn't configure during power up
Alert (7)	4	1111 1111	**0xFF**	0x0	0x0	0x0					MCU Started Up

Version: 20091109

THUB FPGA Registers

Address	Bit	
0x80	0	Reset serdes_reader state machine (level)
	1	Switch between TCD trigger (0) and internal pulser (1)
	2	Reset DDL state machines (level)
	4,5	pulser frequency: 0 = 1.2 Hz 1 = 19 Hz 2 = 76 Hz 3 = 610 Hz
0x81	0 - 3	set/clear m_all[0..3], which controls Serdes FPGA
	0	clear Serdes FPGA channel FIFO (level)
	1	clear Serdes smif state machine (level)
0x83	0 - 7	event-trigger counter
0x84	0	tcd_busy_n (active low, rd-only)
	1	"Run Active" status (rd-only)
	2	TCD Working
0x85		trigger word [7..0]
0x86		trigger word [15..8]
0x87		trigger word [19..16]. Read also issues rd_req to FIFO
0x91		Serdes Register A
	0 - 3	Turn on Serdes Channel [0 .. 3]
	4	switch between test data (0) and "real" data (1)
	7	Data word is geographical data
0x92		Serdes Register B
…		…
0x98		Serdes Register H
0x99	any	Bunch Reset (pulse)