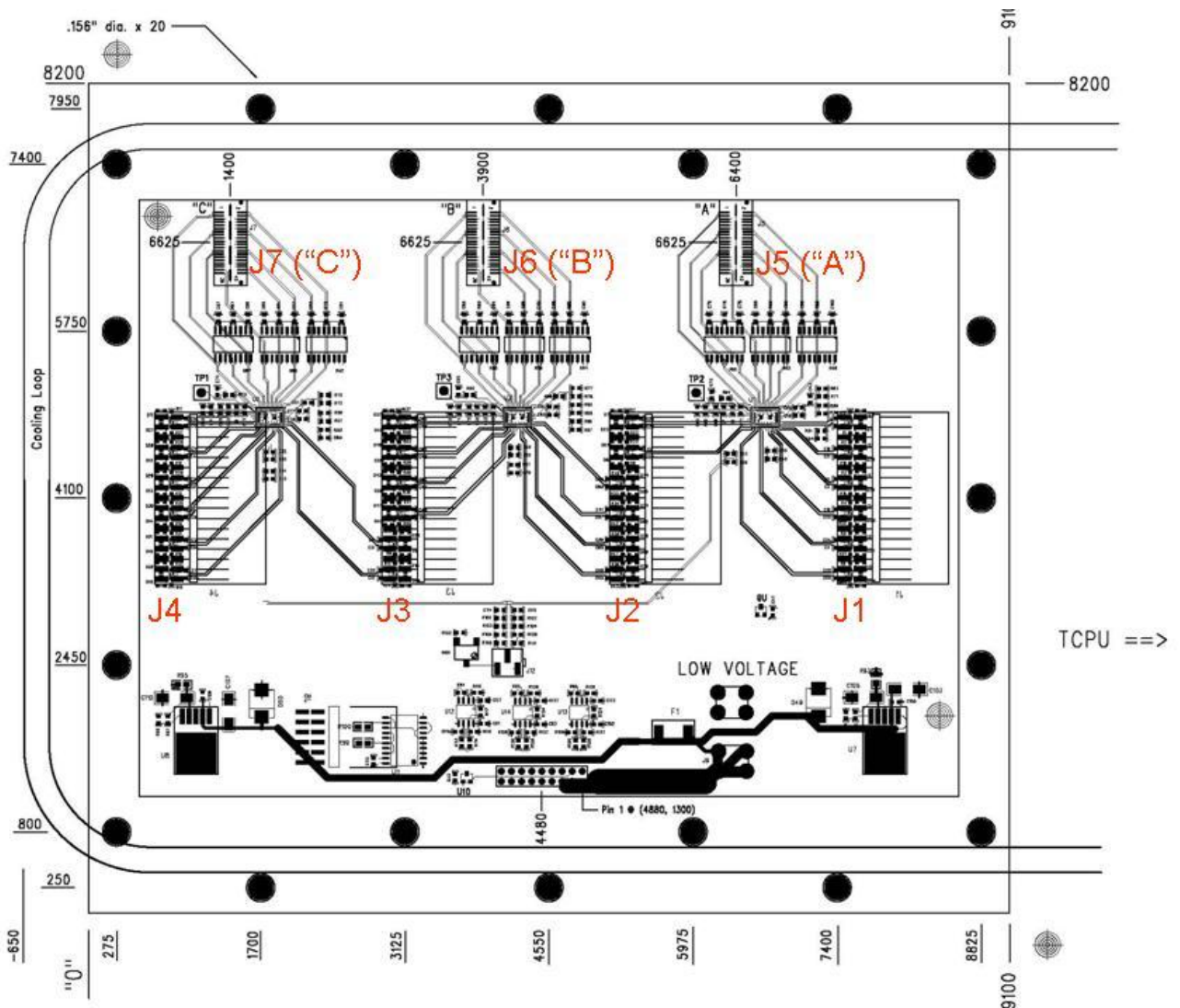


“TINO_N” – “TDIG-E” Mapping

Version: 6, February 14, 2007

This document is based on the alternative mapping suggested by G. Eppley, which was finally implemented on TDIG_E.

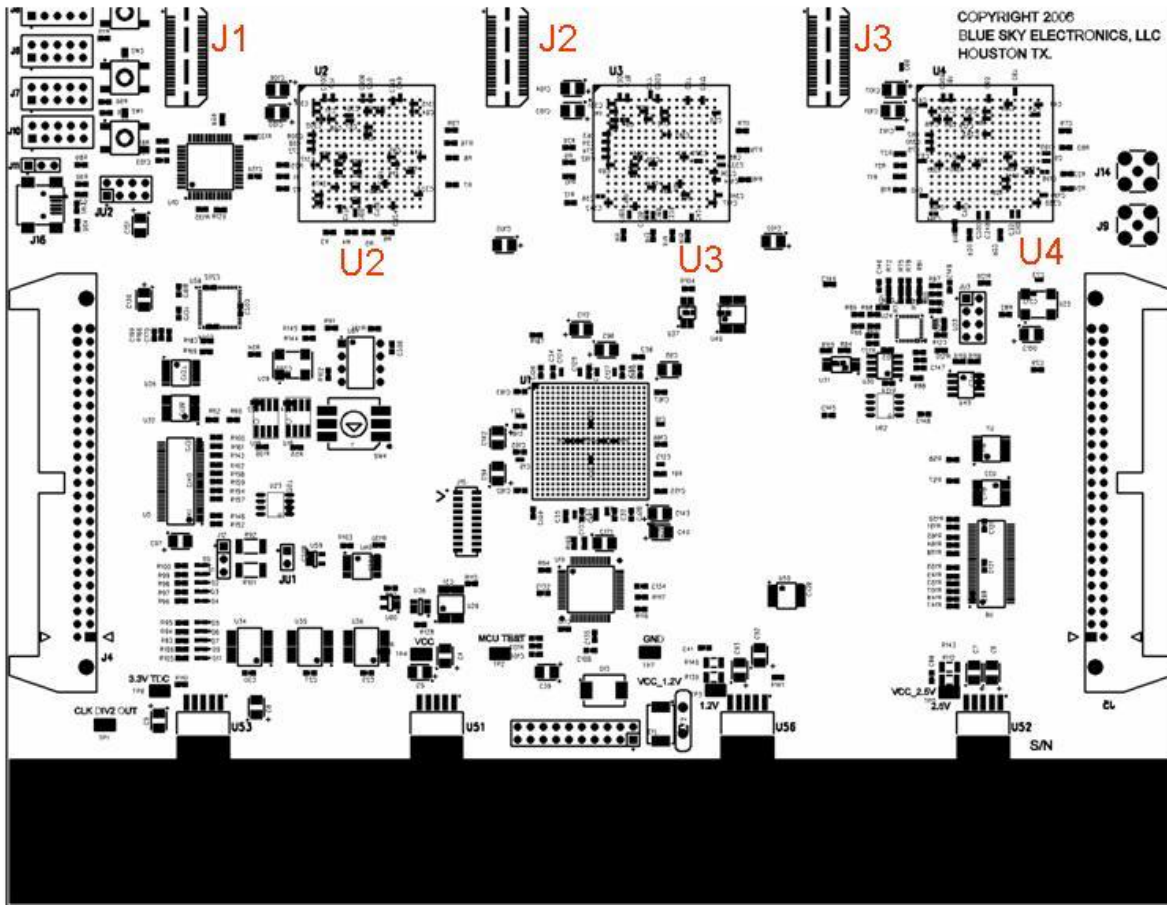
TINO_N has four connectors on the bottom of the board (J1 – J4) that connect to four MRPCs. On the top of the board are three signal connectors that mate with corresponding connectors on TDIG plus one connector for the power. The following picture shows the layout of these connectors as seen when looking at TINO_N from the top.



The MRPC connectors on the bottom of TINO_N are labeled “J1”, “J2”, “J3”, and “J4”. “J4” is the connector closest to eta = 0 (away from TCPU), “J1” is the connector closest to eta = 1 (towards TCPU).

The signal connectors are labeled J5 (“A”), J6 (“B”), and J7 (“C”). J7 (“C”) is the connector closest to eta = 0 (away from TCPU), while J5 (“A”) is the connector closest to eta = 1 (towards TCPU).

TDIG-E has 3 signal connectors on the bottom side of the board (J1, J2, J3) corresponding to the signal connectors on the top side of TINO_N, and a power connector on the bottom of the board (J13) corresponding to the power connector on top of TINO_N. The layout of these connectors as seen when looking at TDIG-E from the top is shown in the following picture.



BLUE SKY ELECTRONICS, LLC TDIG-D DD. ACDI FILE# 2455

SOLDERMASK (TOP)

SOLDERMASK (BOTTOM)

SST (SILKSCREEN TOP) SSD (SILKSCREEN BOTTOM)

The signal connectors on TDIG-E are labeled “J1”, “J2”, and “J3”. “J1” is the connector closest to $\eta = 0$ (away from TCPU), while “J3” is the connector closest to $\eta = 1$ (towards TCPU). “J1” on TDIG-E mates with J7 (“C”) on TINO_N, “J2” on TDIG-E with J6 (“B”) on TINO_N and “J3” on TDIG-E with J5 (“A”) on TINO_N. TDIG-E has three HPTDC chips on top, labeled “U2”, “U3”, and “U4”. “U2” is the chip closest to $\eta = 0$, while “U4” is the chip closest to $\eta = 1$.

The signal path is then intended to be as follows:

MRPC	PAD #	TINO Bottom connector	Pins	TINO top connector	Pins	TDIG Connector	Pins	TDC	Ch
MRPC 1	1	J4	1,2,3,4	J7 ("C")	1,3	J1	1,3	U2	7
	2	J4	7,8,9,10	J7 ("C")	13,15	J1	13,15	U3	7
	3	J4	13,14,15,16	J7 ("C")	25,27	J1	25,27	U2	0
	4	J4	19,20,21,22	J7 ("C")	37,39	J1	37,39	U3	2
	5	J4	25,26,27,28	J7 ("C")	38,40	J1	38,40	U2	5
	6	J4	31,32,33,34	J7 ("C")	26,28	J1	26,28	U3	6
MRPC 2	1	J3	1,2,3,4	J6 ("B")	1,3	J2	1,3	U4	7
	2	J3	7,8,9,10	J6 ("B")	13,15	J2	13,15	U2	4
	3	J3	13,14,15,16	J6 ("B")	25,27	J2	25,27	U4	4
	4	J3	19,20,21,22	J6 ("B")	37,39	J2	37,39	U2	2
	5	J3	25,26,27,28	J7 ("C")	2,4	J1	2,4	U3	3
	6	J3	31,32,33,34	J7 ("C")	14,16	J1	14,16	U2	6
MRPC 3	1	J2	1,2,3,4	J5 ("A")	1,3	J3	1,3	U3	0
	2	J2	7,8,9,10	J5 ("A")	13,15	J3	13,15	U4	2
	3	J2	13,14,15,16	J6 ("B")	2,4	J2	2,4	U2	3
	4	J2	19,20,21,22	J6 ("B")	14,16	J2	14,16	U4	3
	5	J2	25,26,27,28	J6 ("B")	26,28	J2	26,28	U2	1
	6	J2	31,32,33,34	J6 ("B")	38,40	J2	38,40	U4	6
MRPC 4	1	J1	1,2,3,4	J5 ("A")	2,4	J3	2,4	U4	0
	2	J1	7,8,9,10	J5 ("A")	14,16	J3	14,16	U3	5
	3	J1	13,14,15,16	J5 ("A")	26,28	J3	26,28	U4	1
	4	J1	19,20,21,22	J5 ("A")	38,40	J3	38,40	U3	4
	5	J1	25,26,27,28	J5 ("A")	37,39	J3	37,39	U4	5
	6	J1	31,32,33,34	J5 ("A")	25,27	J3	25,27	U3	1

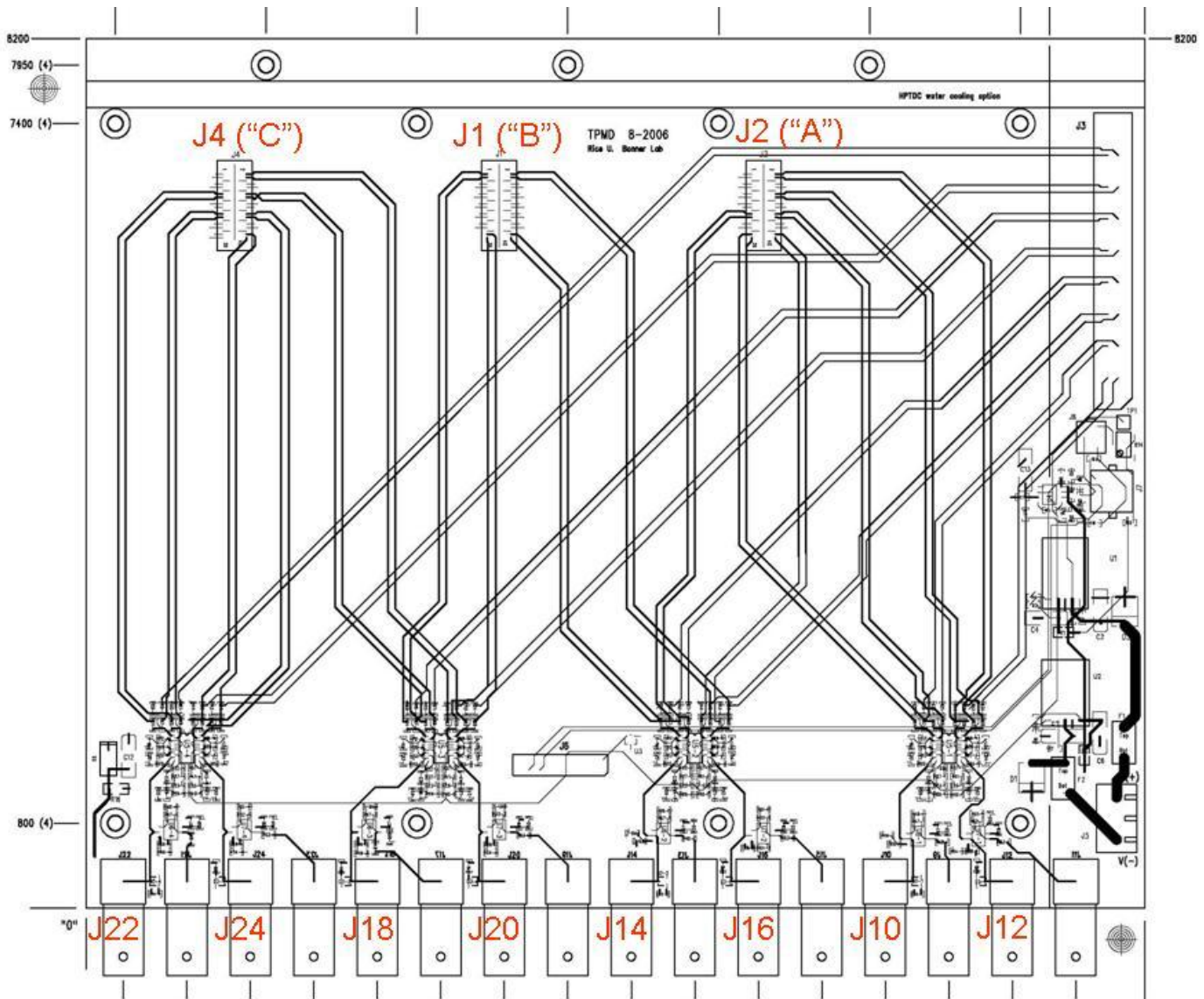
This results in the following connections between the signal connectors on TDIG-E and the HPTDC's on TDIG-E:

TDIG Connector	Pins	TDC	Ch	TINO top connector	Pins	TINO Bottom connector	Pins	MRPC	PAD #
J1	1,3	U2	7	J7 ("C")	1,3	J4	1,2,3,4	MRPC 1	1
J1	2,4	U3	3	J7 ("C")	2,4	J3	25,26,27,28	MRPC 2	5
J1	13,15	U3	7	J7 ("C")	13,15	J4	7,8,9,10	MRPC 1	2
J1	14,16	U2	6	J7 ("C")	14,16	J3	31,32,33,34	MRPC 2	6
J1	25,27	U2	0	J7 ("C")	25,27	J4	13,14,15,16	MRPC 1	3
J1	26,28	U3	6	J7 ("C")	26,28	J4	31,32,33,34	MRPC 1	6
J1	37,39	U3	2	J7 ("C")	37,39	J4	19,20,21,22	MRPC 1	4
J1	38,40	U2	5	J7 ("C")	38,40	J4	25,26,27,28	MRPC 1	5

J2	1,3	U4	7	J6 ("B")	1,3	J3	1,2,3,4	MRPC 2	1
J2	2,4	U2	3	J6 ("B")	2,4	J2	13,14,15,16	MRPC 3	3
J2	13,15	U2	4	J6 ("B")	13,15	J3	7,8,9,10	MRPC 2	2
J2	14,16	U4	3	J6 ("B")	14,16	J2	19,20,21,22	MRPC 3	4
J2	25,27	U4	4	J6 ("B")	25,27	J3	13,14,15,16	MRPC 2	3
J2	26,28	U2	1	J6 ("B")	26,28	J2	25,26,27,28	MRPC 3	5
J2	37,39	U2	2	J6 ("B")	37,39	J3	19,20,21,22	MRPC 2	4
J2	38,40	U4	6	J6 ("B")	38,40	J2	31,32,33,34	MRPC 3	6
J3	1,3	U3	0	J5 ("A")	1,3	J2	1,2,3,4	MRPC 3	1
J3	2,4	U4	0	J5 ("A")	2,4	J1	1,2,3,4	MRPC 4	1
J3	13,15	U4	2	J5 ("A")	13,15	J2	7,8,9,10	MRPC 3	2
J3	14,16	U3	5	J5 ("A")	14,16	J1	7,8,9,10	MRPC 4	2
J3	25,27	U3	1	J5 ("A")	25,27	J1	31,32,33,34	MRPC 4	6
J3	26,28	U4	1	J5 ("A")	26,28	J1	13,14,15,16	MRPC 4	3
J3	37,39	U4	5	J5 ("A")	37,39	J1	25,26,27,28	MRPC 4	5
J3	38,40	U3	4	J5 ("A")	38,40	J1	19,20,21,22	MRPC 4	4

TPMD Mapping

TPMD has 16 BNC connectors mounted on top and on the bottom of the board. The top mounted BNC connectors are labeled “J10”, “J12”, “J14”, “J16”, “J18”, “J20”, “J22”, and “J24”. There are three signal connectors on top of TPMD labeled “J2” (“A”), “J1” (“B”), and “J4” (“C”). The layout of these connectors as seen when looking at TPMD from the top is shown in the following picture:



The resulting mapping from the BNC connectors on TPMD to the TDIG connectors and TDIG’s HPTDC chips is shown in the following table. There are a total of 8 leading edge mappings (“L.E.”) and 8 trailing edge mappings (“T.E.”) for each input BNC connector. The leading edge signals are mapped to two HPTDC with 5 channels on U2 and 3 channels on U4, while the trailing edge signals are mapped to HPTDC U3 with 6 channels and U4 with 2 channels. If we configure U2 and U4 as leading edge, while configuring U3 as trailing edge, this leaves us the shaded channels to use for the start detector:

BNC in	TPMD top connector	Pins	TDIG connector	L.E. TDC	Ch	TPM top connector	Pins	TDIG connector	T.E. TDC	Ch
J10	J2, "A"	26,28	J3	U4	1	J2, "A"	37,39	J3	U4	5
J12	J2, "A"	2,4	J3	U4	0	J2, "A"	14,16	J3	U3	5
J14	J1, "B"	38,40	J2	U4	6	J2, "A"	25,27	J3	U3	1
J16	J1, "B"	2,4	J2	U2	3	J2, "A"	38,40	J3	U3	4
J18	J4, "C"	14,16	J1	U2	6	J1, "B"	1,3	J2	U4	7
J20	J1, "B"	37,39	J2	U2	2	J4, "C"	2,4	J1	U3	3
J22	J4, "C"	25,27	J1	U2	0	J4, "C"	13,15	J1	U3	7
J24	J4, "C"	38,40	J1	U2	5	J4, "C"	26,28	J1	U3	6