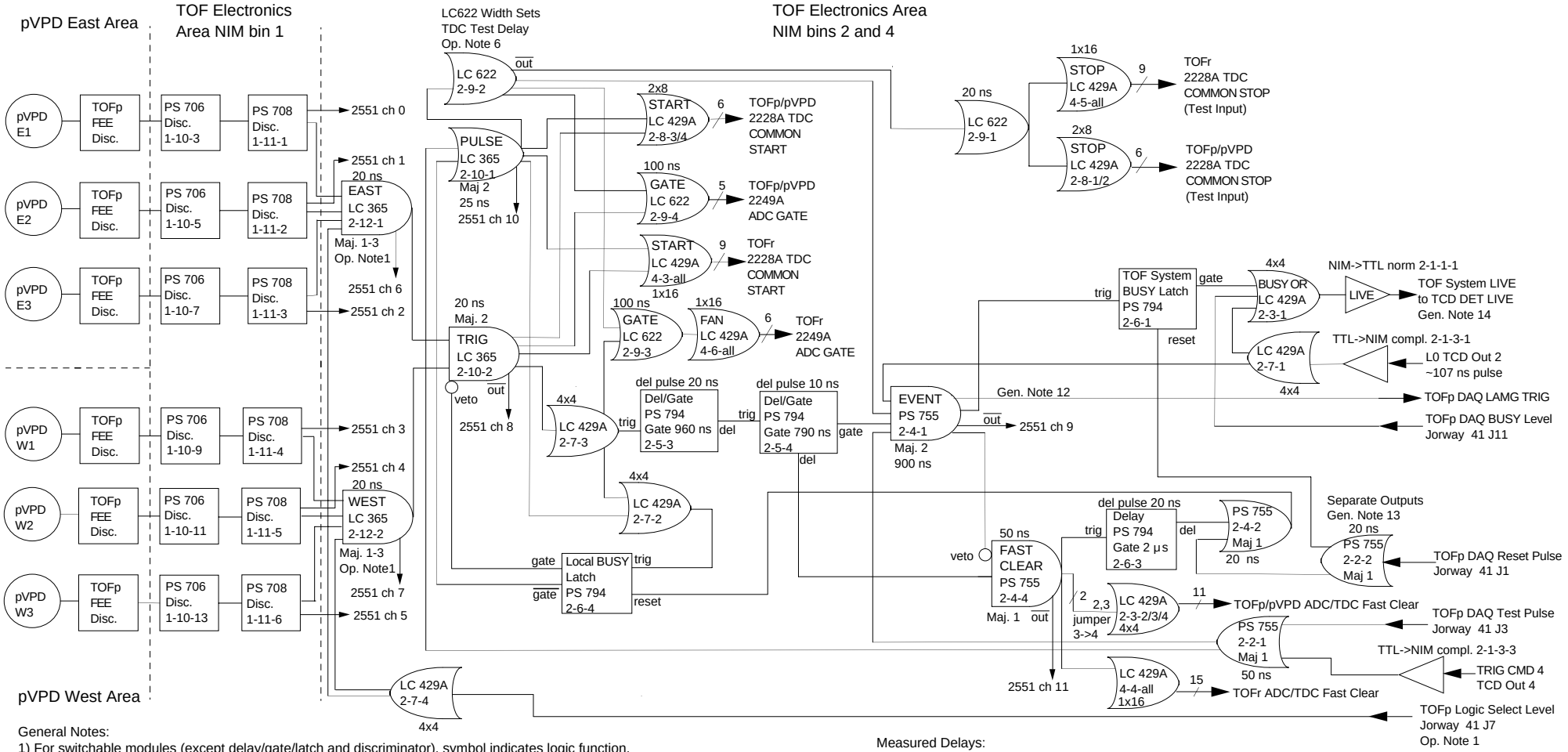

General Notes:
1) For switchable modules (except delay/gate/latch and discriminator), symbol indicates logic function.
2) Discriminator, delay/gate, or latch function indicated in box symbol.
3) Logic element locations in NIM bin are identified by (bin-slot-section) except LC 688AL listed as (bin-slot-section-channel).
4) Delay durations (gate widths) for delay/gate generators are given in box symbol.
5) Output pulse widths are shown for all pulse-forming modules.
6) Connections from logic to LeCroy 2551 CAMAC scaler are indicated.
7) LC 429A logic fans are used where 100% duty-cycle fan-in or fan-out is required. Switch settings are noted.
8) All NIM->TTL and TTL->NIM conversions use LC 688AL.
9) Cable delays (~20 ns) are used from TRIG to TOFp/pVPD GATE and TRIG to TOFp/pVPD and TOF r STARTs.
10) PS 706 (1-10-x) is line receiver and supplies pVPD TDC STOPs via cable delay.
11) PS 708 (1-11-x) is fast fan-out for logic and 2551 scaler.
12) Output to LAMG paired with termination.
13) Outputs separated to avoid reset of one latch also resetting other during testing. Latches are normally reset simultaneously.
14) TOF logic generates a BUSY signal that is inverted in NIM->TTL converter to give LIVE signal for TCD.

Operational Notes:
1) Majority levels of EAST and WEST coincidences are 1-3 depending on selectivity required. Majority level reduces by one if Logic Select line is asserted.
2) Reset Pulse clears the Local BUSY and TOF System BUSY latches unless Reset Control is asserted. If Reset Control is asserted, Reset Pulse only clears the Local BUSY latch.
3) Reset Control must be cleared (set to 0) for pedestal runs.
4) Reset Pulse must be sent by TOFp DAQ at run initialization, L2, abort, and after timeout. For L2 and abort, reset is only sent if trigger token corresponds to L0 token.
5) TOFp DAQ BUSY (Jorway 41 J11) must be asserted during BiRa 2601 readout.
6) Width of LC 622 (2-9-2) sets Start-Stop delay for TDC tests. Delay is 622 pulse width (measured at 400 mV) plus 23.5 ns.

Measured Delays:
1) TCD to (from) TOFp Logic 688AL: 26 ns
2) PS706 (1-10-x) out to LC429A TRIG FAN (2-7-3) out: 48 ns
3) PS706 (1-10-x) out to LC429A TOFp/pVPD START FAN (2-8-3/4) out: 66 ns
4) PS706 (1-10-x) out to LC622 TOFp/pVPD GATE (2-9-4) out: 73ns
5) PS706 (1-10-x) out to LC429A TOFr START FAN (4-3-all) out: sec. 1 - 65 ns; sec. 4 - 66 ns
6) PS706 (1-10-x) out to LC622 TOFr GATE FAN (4-6-all) out: 73 ns
7) TDC test Start-Stop (as of 12/16/02 see Note Op. 6): 50 ns

LeCroy 2551 Scaler Inputs:
0 - pVPD E1
1 - pVPD E2
2 - pVPD E3
3 - pVPD W1
4 - pVPD W2
5 - pVPD W3
6 - EAST (coincidence)
7 - WEST (coincidence)
8 - TRIG
9 - EVENT
10 - Pulser
11 - Fast Clear

TOF Local Trigger
16 December 2002
John W. Mitchell