pVPD East Area

TOFp Electronics Area

pVPD E1 — TOFp FEE Disc. — PS 708 Disc.

pVPD E2 — TOFp FEE Disc. — PS 708 Disc.

pVPD E3 — TOFp FEE Disc. — PS 708 Disc.

EAST LC 365 12-1 — Maj. 3

LC 622 9-2

PULSE LC 622 9-1

START LC 429A 8-3/4 — 6 — 2228A TDC COMMON START

GATE LC 622 9-4 — 4 — 2249A ADC GATE

Del/Gate PS 794 50 ns 6-2 — del — STOP LC 429A 8-1/2 — 6 — 2228A TDC COMMON STOP (TEST Input)

Maj. 2

TRIG LC 365 10-2 — veto

Del/Gate PS 794 575 ns 5-1 — st — del

Del/Gate PS 794 215 ns 5-2 — del

LC 429A 7-1 — set

TOF System BUSY Latch PS 794 6-1 — out — clr

BUSY OR LC 429A 3-1

TTL->NIM compl. 1-2-3 — Pulser from TCD J3

NIM->TTL compl. 1-1-1 — TOF System BUSY to TDC DAQ BUSY

TTL->NIM compl. 1-2-1 — L0 from TCD J1

PS 755 4-1 300 ns

Del/Gate PS 794 839 ns 5-3 — st — del

Del/Gate PS 794 215 ns 5-4 — gate — del

EVENT PS 755 4-3 Maj. 2 300 ns

PS 755 2-1 Maj 1

TOFp DAQ LAMG TRIG IN

TOFp DAQ BUSY Level Jorway 41-2 J3

PS 755 2-3 Maj 2 — TOFp DAQ Pulser Enable Level Jorway 41-2 J1

LC 429A 7-3

LC 429A 7-2

Local BUSY Latch PS 794 6-4 — set — out — clr

FAST CLEAR PS 755 4-4 Maj. 1 — veto

Delay PS 794 2 μs 6-3 — st — del

PS 755 4-2

PS 755 2-2 Maj 1 — TOFp DAQ Reset Pulse Jorway 41-1 J1

LC 429A 3-2/3/4 — 10 — ADC/TDC Fast Clear

PS 755 2-1 Maj 1 — TOFp DAQ Test Pulse Jorway 41-1 J3

WEST LC 365 12-1 — Maj. 3

pVPD W1 — TOFp FEE Disc. — PS 708 Disc.

pVPD W2 — TOFp FEE Disc. — PS 708 Disc.

pVPD W3 — TOFp FEE Disc. — PS 708 Disc.

pVPD West Area

LC 429A 3-1 — TOFp Logic Select Level Jorway 41-2 J5

TOFp Local Trigger
Planned Configuration
Drawn 25 April 2001
John W. Mitchell

Notes:
1) For switchable modules (except delay/gate/latch and discriminator), symbol indicates logic function used here.
2) Discriminator, delay/gate, or latch function written in box symbol.
3) LC 429A logic fans used if 100% duty-cycle fan-in or fan-out is required.
4) Pulse forming modules (LC 622, PS 755) used to convert level to pulse at leading edge.
5) Logic element locations in NIM bin are identified by (slot-section) except LC 688AL listed as (slot-section-channel).
6) All NIM->TTL and TTL->NIM conversions use LC 688AL NIM Slot 1.
7) Two Jorway 41 output registers are assumed to eliminate confusion between pulses (Reset and Pulse) and levels (Pulse-Enable, TOFp DAQ BUSY, and Logic Select).
8) Majority levels on EAST and WEST logic elements may be 2 or 3 depending on selectivity rquired. Normal majority level is 3, but reduces to 2 if Logic Select line is asserted.
9) Reset clears the Local BUSY latch in normal running and both the Local Busy and TOF System BUSY latches in pulse-enabled running. Reset must be sent by TOFp DAQ at run initialization, L2, abort, and after timeout. For L2 and abort, reset is only sent if trigger token corresponds to L0 token.
10) The Pulse-Enable level is set to 1 for runs in which STAR pulser triggers are expected.
11) Provision is made for a software TOFp DAQ BUSY.