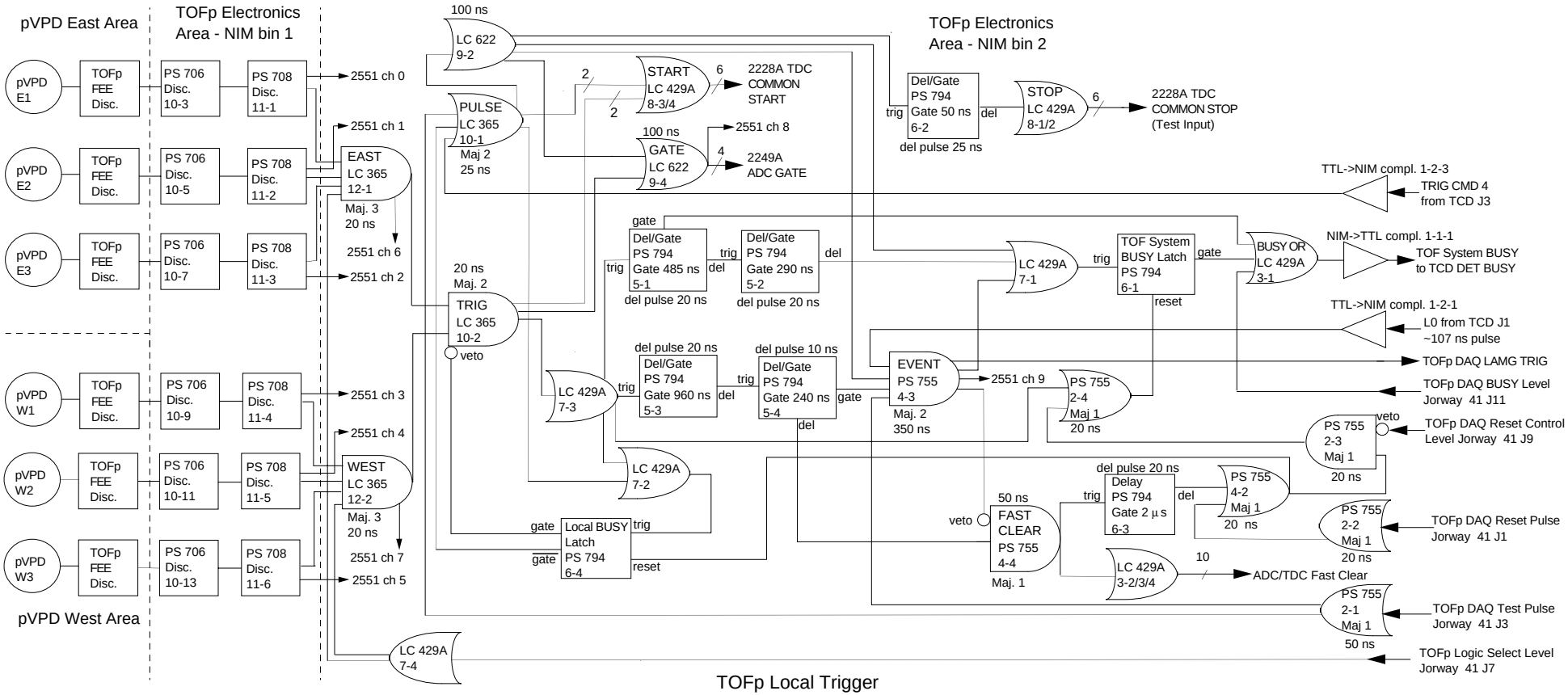


TOFp Local Trigger
5 July 2001
John W. Mitchell

General Notes:
1) For switchable modules (except delay/gate/latch and discriminator), symbol indicates logic function.
2) Discriminator, delay/gate, or latch function indicated in box symbol.
3) Logic element locations in NIM bin are identified by (slot-section) except LC 688AL listed as (slot-section-channel).
4) Delay durations (gate widths) for delay/gate generators are given in box symbol.
5) Output pulse widths are shown for all pulse-forming modules.
6) Connections from logic to LeCroy 2551 CAMAC scaler are indicated.
7) LC 429A logic fans are used where 100% duty-cycle fan-in or fan-out is required.
8) All NIM->TTL and TTL->NIM conversions use LC 688AL.

Operational Notes:
1) Majority levels of EAST and WEST coincidences are 2 or 3 depending on selectivity required. Normal majority level is 3, but reduces to 2 if Logic Select line is asserted.
2) Reset Pulse clears the Local BUSY and TOF System BUSY latches unless Reset Control is asserted. If Reset Control is asserted, Reset Pulse only clears the Local BUSY latch.
3) Reset Control must be cleared (set to 0) for pedestal runs.
4) Reset Pulse must be sent by TOFp DAQ at run initialization, L2, abort, and after timeout. For L2 and abort, reset is only sent if trigger token corresponds to L0 token.
5) TOFp DAQ BUSY (Jorway 41 J11) must be asserted during BiRa 2601 readout.

Measured Delays:
1) TCD to (from) TOFp Logic 688AL - 26 ns
2) PS706 line-receiver output to LC429A TRIG FAN (7-3) output - 48 ns
3) PS706 line-receiver output to LC429A START FAN (8-3/4) output - 48 ns
4) PS706 line-receiver output to LC622 GATE (9-4) output - 55 ns

LeCroy 2551 Scaler Inputs:
0 - pVPD E1
1 - pVPD E2
2 - pVPD E3
3 - pVPD W1
4 - pVPD W2
5 - pVPD W3
6 - EAST (coincidence)
7 - WEST (coincidence)
8 - TRIG (from ADC GATE)
9 - EVENT
10 - CLOCK (to be installed)
11 - GATED CLOCK (to be installed)