CDB_CSR_revI.doc :: CTB CDB control and status registers:

RHM 9/2/98
REV B revised 10/20/98 RHM
REV C 1/14/90 RHM added individual disc. timing
Rev D 3/15/99 RHM updated for 8th bit
Rev E   3/16/99 RHM updated for 4 bit disc delay and msb/lsb order
Rev F 12/3/99 RHM modified for Prom version 3.0 – read write addresses offset by 0x40
Rev G 1/27/00 LG added command to fire LED pulser, formatting.
Rev H 1/31/00 LG added comments
Rev I 2/4/00 LG updated addresses for 32 bit reads and writes. Added comments

DESCRIPTION:

All communication to and from the cards is via VME 32 bit reads and writes. Memory mapped I/O is used for all functions. Written registers do NOT return the written data when read.

Board select is via the top 8 bits of the 32 bit address field for selection of each of the 17 cards in the crate. Address are; (in CTB Crate; 0x10000000 to 0x20000000) see STAR Trigger VME Base address document.

Writes to the cards (32 bit) set 16 bit registers for timing control. Single writes set multiple parameters in 3 and 4 bit groups for timing.

Writes of any value to two addresses cause 8th bit switch to be set for Integrator or Discriminator data to be included in data.

A single write to the card (32 bit) sets the LED mask. Each of the lower 16 bits sets one LED enable line. There is no decoding of the word.

Reads from the cards read out data stored in FIFOs during LED pulser events. Up to 64 - 8 bit values are stored in each of 16 FIFOs and are read out by reading the same location multiple times. Each channel has a unique address.

All transfers are 32 bits wide. There are no 16 bit transfers. P1 and P2 on VME are used. All transfers are simple reads and writes.

The LED pulser can be fired on a board by board basis with a write of any value to a particular address.

The board VME interface has been tested with 68040 and PPC604 based processors.

CTB CDB control and monitoring

Memory Map:

Board level functions:

Function:	Address offset from board select:
RHIC strobe phase and Discriminator Timing	xxxxxx40
LED mask	xxxxxx44
Discriminator threshold DAC	xxxxxx48
8th bit switch on	xxxxxx4c
8th bit switch off	xxxxxx50
Fire LED Pulser	xxxxxx54

(note: to fire the LED pulser using the VxWorks "m" command; type "m 0x??000054, 4" where ?? is the board base address. When you get the Vxworks address prompt, type "1" and return. This will fire the LED pulser on that board.)

Channel level functions:

Function:	Address offset from board select
Integrator and disc. Timing	xxxxxx00 – xxxxxx3c for channel 0 to 15.
Fifo readout	xxxxxx60 – xxxxxx9c for channel 0 to 15.

Board based controls:

RHIC strobe phase (2.5 nsec steps) and discriminator timing (5 nsec steps): write one 16 bit word (xxxxxx40)

MSB 15 14 13 12 | 11 10 9 | 8 7 6 | 5 4 3 | 2 1 0 LSB
   | x x x x | d_stop | d_start | out-latch | RS delay |

LED mask: write one 16 bit word (xxxxxx44)

MSB   15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 LSB
enable channel 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Discriminator threshold DAC level set: write one 8 bit word (xxxxxx48)

range from 0 to 2.45 Volts
MSB| 7 6 5 4 3 2 1 0 LSB
    | DAC level |

8thbit switch on: write one 8 bit word (xxxxxx4c)

Changes LSB in data from Integrator LSB .
MSB 7 6 5 4 3 2 1 0 LSB
    x x x x x x x x any value is ok

8thbit switch off: write one 8 bit word (xxxxxx50)

Changes LSB in data from gated Discriminator output.
MSB 7 6 5 4 3 2 1 0 LSB
    x x x x x x x x any value is ok

Fire LED pulser command : write to one 16 bit word (xxxxxx54)

Fires LED pulser for that board.
MSB 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 LSB
    x x x x x x x x x x x x x x x any value

Channel based controls and monitoring:

16 channels per card

Controls:

Integrator timing (10nsec steps for Integrator start and stop. Discriminator delay is 5nsec steps: one 16 bit word per channel (xxxxxx00 – xxxxxx3c)

MSB 15   14   13   12 |11 10 9   8 | 7 6 | 5   4   3 | 2   1   0 LSB
    | x   x   x   x | disc delay | x x | Int_stop | Int_start |

Monitoring:

LED event data store: 16 channels each 64 deep maximum 8 bit FIFOs (xxxxxx60 – xxxxxx9c)

Currently 21 samples are the default.

        MSB| 7 6 5 4   3   2   1   0 LSB
DATA MSB| 7 6 5 4   3   2   1   0 LSB