STAR TAC Module Theory of Operation

required inputs:

1) PECL clock = RHIC strobe ~ 9.4MHz (duty cycle matters!)
on pins 1&2 of front-panel JP2 (located at bottom of module)
Note: This input is NOT terminated internally; must be terminated at end of multidrop cable.
2) +5V @ 6A via VME P2 Note: this is a "back-of-crate" card spanning P2 and P3
3) ECL inputs from PMT Discriminators on JP1

outputs:

1) copy of inputs (PECL) on JP3 stretched to be at least 50ns for Scalers
starts with leading edge of discriminator input signal,
ends with *trailing* edge of delayed RHIC Strobe (which is why duty cycle matters)

2) gated current source LEMOs 1-16 top to bottom
(current level set by pot located near U84 (nominal setting -5.58V on U84 pin 4)
resulting in an output amplitude of 12ma or 600mV into 50 ohms = 12pc per ns to ADC
starts with leading edge of discriminator input signal
ends with *leading* edge of delayed RHIC strobe
note: must end before close of downstream ADC gate
note: earlier starts make larger signals.

3) "monitor start 16" = 10% sample of stretched discriminator #16 signal LEMO 17 from top

4) "monitor stop" = 10% sample of delayed RHIC strobe; LEMO 18 from top

5) "analog sum" LEMO 19 from top
each stretched discriminator signal contributes -1.4ma into a 50 ohm load (or -70mV)
adj pot near U89 for zero output (into 50 ohms) with no inputs

other adjustments:

front-panel jumpers to set delay of RHIC strobe.(in 3ns steps)
see labels on PCB; max = (32+16+8+4+2+1)x3ns = 189ns = nonsense. Typical = 16x3ns = 48ns