October 20, 1998 LG, RM
DRAFT

CDB Testing Plans

CDB Functional Areas :

- 16 channel input on Standard 9U VME hardware.
- 16 Gated integrators with individually adjustable start and stop timing.
- 16 discriminators for time-based rejection with individually adjustable start and stop timing.
- 16 channels of ADC for digitization with timing remotely adjusted.
- Latching for the output(s) of the ADC(s).
- Logic circuitry to use the 8^{th} ADC bit as a timing indicator for peripheral collisions (remotely switched). All channels will be in the same mode on each card.
- LED driver system with individual channel masking but simultaneous operation at fixed level.
- Temporary store for trapping of LED signal (read out by Slow Controls).
- Slow control interface for control and monitoring via VME.
- Analog monitor and gate timing monitor outputs.
- ECL discriminator monitor outputs.
- Power fuses.

Quantity:
20 16 ch. 9U VME boards (including spares)

Testing plans;
The low quantity of finished boards (20 including spares) indicates that this task does not merit the investment of time required to develop an automated testing station. The testing of the production boards is expected to be done with standard test equipment; pulsers, logic analyzers, etc. We will test all of the functional areas listed above for each channel on each board. We outline a procedure below;

Individual board tests;

1. Apply power, note current draw.
2. Plug into VME crate, write and read CSR.
3. At standard setting apply input pulse and read ADC value from P3
4. Apply pulser ramp synchronized with RHIC strobe and move ADC gate looking for corresponding increase and decrease in ADC values read via VME from temporary store.
5. Set discriminator threshold and look for discriminator output.
6. Set time window and enable timing 8^{th} bit. Adjust input and window and test functionality.

7. Sequentially attach board channel ADC inputs and LED outputs to CTB tray.
8. Activate LED pulser, look for appropriate data.
9. Check gate and PMT test points on front panel.

System level tests.

1. Begin with a crate of 17 CDB boards, VME processor
2. Test TCD functionality; RHIC strobe, LED pulser special event
3. Check Led pulser event flag.
4. Use slow controls software to set up boards and read data.
5. Use P3 to connect CDB to DSMI to DSM and check that latching, phase adjust, etc. give proper data flow to DSM.