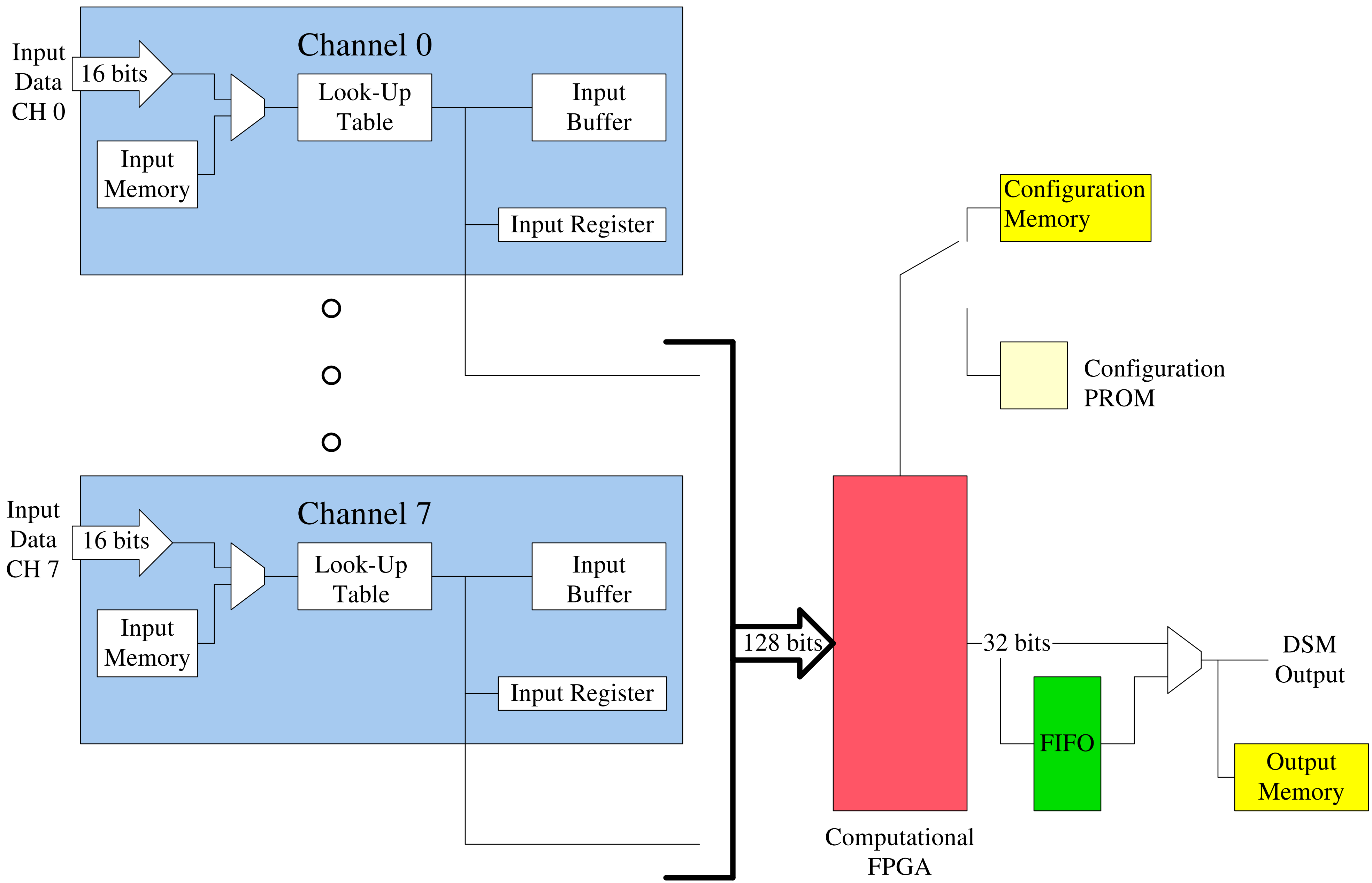

Channel 0
Input
Data
CH 0
16 bits
Look-Up
Table
Input
Buffer
Input
Memory
Input Register
Channel 7
Input
Data
CH 7
16 bits
Look-Up
Table
Input
Buffer
Input
Memory
Input Register
128 bits
Configuration
Memory
Configuration
PROM
Computational
FPGA
32 bits
FIFO
DSM
Output
Output
Memory