Test for Trigger Control Unit (TCU) boards for STAR Trigger Level 0 (preliminary draft)

1. Requirement: Test of the Trigger Word (TrWd) Look-Up Table (LUT).
   Justification: TrWd LUT takes 12 bit DSM input and 6 bit modified busy and outputs 16 bit TrWd plus 1 bit Priority Event flag and 1 bit Contamination Event flag.
   Implementation: Define a TrWd LUT and run input stream of 12 bit numbers, 0-2^12, with the 6 modified busy bits set to 0. Test output of TrWd LUT. The contamination bit should be set whenever there are TPC events within the drift time if TPC. The Priority bit should be set whenever there is a TPC event. Give modified busy bits non-zero values and test TrWd LUT output.

2. Requirement: Test of Information and Priority Information FIFO 2b.
   Justification: DSM input is stored in Information FIFO's.
   Implementation: Input as in 1 above, and test to see that when Priority bit is 1, the DSM input is written to Priority Information FIFO 2b, or the information FIFO 2b in the appropriate address space.

3. Requirement: Test of Prescale Counters.
   Justification: 20 bit Prescale Counter is updated upon input of 16 bit TrWd and FPGA Prescaler Controller compares that to Prescale Table. If -Trigger is Dead- Flag is not set, Trigger flag is set by Controller.
   Implementation: Load pre-scale factor for each 16-bit TrWd and test that the Trigger Flag is set when stream of data is input and the required number of TrWds are accumulated for each TrWd. Test that wide range of pre-scale factors work.

4. Requirement: Test Action Word (AW) LUT.
   Justification: For 16 bit TrWd input, AW LUT outputs 16 bit AW and sets TPC busy flag.
   Implementation: Define an AW LUT and for an input stream of numbers, 0-2^16, check 16 bit AW for each input to check that correct AW corresponds to appropriate input. Check that TPC busy bit is set for correct input.

5. Requirement: Test the Token and Priority Token FIFO’s
   Justification: Tokens are filled with 12 bit which are combined in the output with the AW.
   Implementation: Input 100 Tokens in Token FIFO and allow tokens to run out to check busy. Check that Token from Priority Token FIFO is output when Priority event flag is set.

6. Requirement: Test of the Response FIFO.
   Justification: The TCU stores Token plus AW in Response FIFO as it receives it from Level 1 and Level 2 when the decision is made to abort or accept an event.
   Implementation: From Input stream of 1 above, and send to Response FIFO various abort and accept events, and check when Trigger Flag is false, that appropriate abort or accept is issued to P3.

7. Requirement: Test of Information and Priority Information 1 FIFO.

Justification: The 28 bit Information 1 FIFO's store the 16 bit AW plus 12 bit Token.
Implementation: For input stream of 1, check that AW + Token get stored in appropriate addresses.

8. Requirement: Test of the Accepted Trigger Word Counters 1 and 2.
Justification: Counter used for scaling input from DSM and 6 modified busy bits.
Implementation: Test that counter is incremented for appropriate TrWd when Trigger flag is set. When counter 1 is full, check that counter 2 is then being written and counter 1 being read and zeroed.

9. Requirement: Test of the Information and Priority Information FIFO 3a.
Justification: FIFO's 3a store the 16 bit TW and the Priority and Contamination Flags.
Implementation: For input from 1 above, check addresses in Information FIF) 3a and Priority Information FIFO 3a, to assure that input is written to appropriate addresses. Check that when priority bit is set, that the input is written to Priority information FIFO, and not the Information FIFO.

10. Requirement: Test of the Simulation Memory.
Justification: Input into TCU can come from either DSM tree or Simulation Memory as loaded by Operation Control (OpCon).
Implementation: Input stream from 1 above from simulation memory.

11. Requirement: Test Information and Priority Information FIFO 3b
Justification: FIFO's 3b store unmodified busy information.
Implementation: For busy bits that are input for 1 above, check that they are written to FIFO 3b in appropriate addresses. Check that when priority bit is set, that input is written to Priority Information FIFO.

12. Requirement: Test Input Counters 1 and 2.
Justification: Counters 1 and 2 track number of 18 bit words from 16 bit DSM input plus 6 bit detector busy.
Implementation: For every non-zero input from 1 above, read Input Counter to assure it is being incremented. When counter 1 is full, check that counter 2 is then being written and counter 1 being read and zeroed.

13. Requirement: Test of the Information and Priority Information FIFO's 2a.
Justification: FIFO's 2a store 16 bit DSM addresses.
Implementation: Write cyclic string of all DSM addresses to FIFO’s. Test that addresses written to correct FIFO when priority bit is set.

14. Requirement: Test FIFO 2a monitor.
Justification: Monitor sets Halt DSM to prevent data in DSM to be overwritten.
Implementation: Using test 13 above, and with a trigger bit being set, check that bit is set in monitor for appropriate DSM address. For trigger bit being continuously set, check that HALT DSM bit is set properly. Check that the monitor bit is cleared from L1/2.

15. Requirement: Test OpCon and Address Control (AdCon) FPGA's.

Justification:
Implementation:

16. Requirement: Test of TCU Interface Board
Justification:
Implementation:

17. Requirement: Test of Latch
Justification:
Implementation: