	only L1 crate	CTB	EEC	all cpus
collision thru L0 -> TCU	~1.5	1.5		1.5
L1 polling on TCU	~2	2		2
L1 read 6 FIFOS	~3	3		3
L1 build evt desc				
L1(HI) to L1(ANA) msg (no myri)				
L1 bookkeep		~36		~36
L1 read L1 DSMs	20			
L1 -> 1 crate (sndmsg)				
L1 -> 2 crates (2 sndmsg)				
L1 -> all crates				
crate msg digestion				
crate read DSMs		20		20
L1 -> L2 w/o crates (myrmem)				
L1 -> L2 w/ L1 crate	55	55		55
1 crate -> L2 (myrmem)		55		
1 crate msg to L2 (sndmsg)		40		
L1 -> L2 w/ all crates				
L1 msg -> L2 (sndmsg)	40	40		
L2 minimum thinking				
L2 event build				
L2 byte swap				
L2 -> DAQ w/o data				
L2 -> w/ 1 token payloed				
L2 -> DAQ w/ 11 token payload				
L2 -> L1 cmd (sndmsg)	40	40		
DAQ -> L2				
L2 -> L1 token release	40	40		
L1 -> TCU token return				
L1->L2->L1 (1 token, no pp)	236	312	305	518
L1->L2->L1 (w/ L2 write, 1 tok, no pp)	241			
L1->L2->L1 (4k tok, 5pp)	223			
L1->L2->DAQ->L1 (1 tok, 0pp)	3226			
L1->L2->DAQ->L1 (1 tok, 5pp)	4167			
L1->L2->DAQ->L1 (4k tok, 5pp)	588			