How to Simulate and Implement DSM Algorithms using ModelSim, Synplify Pro and Lattice Classic

E.G. Judd

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Start with a directory containing just the vhdl code, the constraints files and the do_files

Simulating Your Project – ModelSim

1. Launch Model Sim
2. Click on File -> New -> Project, and select "Yes' to close the current project.
3. In the Create Project dialog box specify the project name. The directory should be the one you just created. Leave the Default Library Name set to "work". Make sure "Copy Library Mappings" is checked, and points to the main modelsim.ini file.
4. In the Add items to the Project dialog box select "Add existing file". Browse to the files in the vhdl subdirectory and select then all.
5. If you use any components from the STAR_Trg_Lib library then click on File -> New -> Library. Make sure "map to an existing library" is checked. Specify the Library Name as STAR_Trg_Lib and then browse to the STAR_Trg_Lib/STAR_Trg_Lib directory.
6. If there is more than one local VHDL file then click on Compile -> Compile order and make sure the files are listed in reverse order, i.e. the top VHDL file should be listed last and lower level components should be listed first.
7. Click on Compile -> Compile All. The Transcript window gives a report. Double click on any red error messages to get the details. Compiled code will automatically be added to the work library.
8. Click on the Library tab. Library "work" should now contain the compiled entities, including the top one. If STAR_Trg_Lib is included then it should also be visible.
9. In the Transcipt window type "vopt +acc top –o top_opt. This will compile the code so you can see all the processes separately, and all the variables inside them.
10. In the Transcript window type "vsim top_opt" to load the design.
11. In the Transcript window type "do do_files/<my do file name>.do" to run your simulation.
12. In the Transcript window type "exit" and click on "Yes" when you are done.
13. NOTE: Sometimes it is desirable to add a new component to STAR_Trg_Lib. Put the vhdl file in the STAR_Trg_Lib/vhdl subdirectory. Open the STAR_Trg_Lib project. Click on Project -> Add to Project -> Existing File and then browse to select the new file. Click on Compile -> Compile order to put it at the correct place in the list. Then right-click on the file name and make sure "Compile to library" is set to STAR_Trg_Lib. Finally, click on Compile -> Compile All.

Synthesizing Your Project – Synplify Pro

1. Start with a directory containing just the vhdl code, the constraints files and the do_files
2. Launch Synplify Pro
3. Close the previous project
4. Use the "File -> New" pull-down menu to create a new Synplify project in the new directory with the name syn_crate_dsm_year_version. Don't click on "File -> New Project" because that menu automatically creates the new project in the old project's directory.
5. Add File to add the local vhdl files. They will show up in the work library
6. Add File again to add all the necessary files from the STAR_Trg_Lib directory. In the Add Files palette remember to specify the VHDL library name is STAR_Trg_Lib.

7. Arrange the VHDL files so that the main entity is at the bottom and all components it instantiates are compiled first. Everything in the STAR_TRG_Lib library should come at the top of the list, again in the appropriate order.
8. Click Implementation Options to select the device (Lattice ORCA Series 2, 2C40A, -4) and specify a frequency of 39.2 MHz (= 25.5ns period)
9. Click Run
10. New File to add a blank syn_crate_dsm_year_version.fdc file in the rev_1 subdirectory
11. Edit the fdc file. Cut and paste all the attributes from the correct (dsmi or tdsmi) constraints file into the fdc file
12. Click on Run
13. Check the report, and then edit the fdc file to remove any constraints for pins that are not being used in this algorithm.
14. Click on Resynthesize All
15. Save and Exit

Implementing Your Project

1. Start Program ispLEVER Classic Project Navigator
2. File->New Project, browse to the main project directory, Project Name '<crate>_<dsm>_<year>_<version>', select Design Entry Type 'EDIF', "Next".
3. Select "Show Obsolete Devices" and then select the or2c40a-4ps304, then "Next"
4. Import the 'rev1/syn_xxx.edn' file into your design:
5. Double-click on "Map Design" in the process window, this will produce a prf constrains file which can be can be edited in the constrains editor
6. Double Click on "Constrains Editor" (takes a while)
7. To set the timing constrains: Select the "Clock" Tab
    a. If it is not shown, enter the "clk_c" in an empty Clock Net field, <Tab><Tab><Tab>
    b. Enter 25.5 in the "Period" field on the same line <Tab>
    c. Enter 12.75 in the "High" field on the same line.<Enter>
8. To relax the timing constrain for a register: Select the "Sync Path" Tab
    a. Click in the "From" field until the pull down menu appears
    b. Select the register component, for example: 'engine_registers/engine_register0(0)'
    c. Click on the "To" field
    d. Select the 'value above threshold' bit which corresponds to this register for example 'reg_ADC_East_above_th'
    e. Click on the "Clock Multiplier" field and enter '10', <Enter>
    f. Click on the "Clock" field and select "clk_c". If "clk_c" is not there, enter it by hand.
    g. Repeat a) to f) for all registers
9. File->Exit, Save "Yes", all constrains are written to the top.prf file
10. Click on Edit Constrains ASCII in the process window
11. A editor with the top.prf file pops-up, go to the bottom of this file
    a. The time constrain can be found under "Period Net…"
    b. The registers are found under "Multicycle"
    c. Replace all explicit bit addresses by a '*' wildcard to make the multicycle valid for all bits of that register.
    d. File->Exit, Save? "Yes"
12. Set the checkpoint properties: Tools->Timing Checkpoint options; disable 'run checkpoint' for both before and after route, or set the options if checkpoint fails to 'continue', "OK"
13. Set Properties for Place and Route Right Click "Place and Route" Change the defaults to: Ignore Preference Errors = False
14. Set Properties for Trace: Tools->Trace Options, "Worst Case Path" to 1000
15. Properties for Bitstream files: Right Click on "Generate Bitstream/Prom data"->Properties
    a. OutPut Format = Bit File (PROM Data)

   b. Output Format = Raw Bit File (.rbt)
   c. Done Signal ->Cycle1
   d. I/O Tri State Release ->Cycle2
   e. Internal Set/Reset Err. ->Cycle 2 (not available ?)
   f. “Close”
16. Steps 1) to here have to be done only during the first run of a project.
17. If the project already exists, Start ispLever, File->Open Project > browse to <my_project_name>/netlist/top.lsp “Open”.
18. Click on BitStream Report. The ispLever Tool will perform all Steps for you.