Xilinx ISE Settings for Compiling QT Algorithms

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Xilinx ISE Version

QT projects need to be implemented using Xilinx ISE version 6.2i with NO Service Packs installed. The process version numbers are therefore:

1) Synthesis: Release 6.2i - xst G.28
2) Translate: Release 6.2i - ngdbuild G.28
3) Map: Release 6.2i Map G.28
4) Place and Route: Release 6.2i Par G.28
5) iMPACT: PROMGEN: Xilinx Prom Generator G.28

The following system environment variables need to be set:

1) set XVKMA_CORE_LUT_PACK=TRUE
2) set XIL_PAR_MAX_PLOAD=100
3) set XIL_GUIDE_CONNECTRPT=1

ISE Settings for QT8b Projects

1) The part number is xc2v500-5fg456
2) Synthesis. NOTE: 4 Items in **RED** are different from the default values

```
=========================================================
*                  Synthesis Options Summary                  *
=========================================================
---- Source Parameters
Input File Name                    : top.prj
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO
Verilog Include Directory          :

---- Target Parameters
Output File Name                   : top
Output Format                      : NGC
Target Device                      : xc2v500-5-fg456

---- Source Options
Top Module Name                    : top
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
FSM Style                          : lut
RAM Extraction                     : Yes
RAM Style                          : Auto
```

ROM Extraction : Yes
ROM Style : Auto
Mux Extraction : YES
Mux Style : Auto
Decoder Extraction : YES
Priority Encoder Extraction : YES
Shift Register Extraction : YES
Logical Shifter Extraction : YES
XOR Collapsing : YES
Resource Sharing : YES
Multiplier Style : auto
Automatic Register Balancing : No

---- Target Options
Add IO Buffers : YES
Global Maximum Fanout : 500
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Equivalent register Removal : NO
Slice Packing : YES
Pack IO Registers into IOBs : auto

---- General Options
Optimization Goal : Speed
Optimization Effort : 2
Keep Hierarchy : NO
Global Optimization : AllClockNets
RTL Output : Yes
Write Timing Constraints : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : maintain
Slice Utilization Ratio : 100
Slice Utilization Ratio Delta : 5

---- Other Options
Read Cores : YES
cross_clock_analysis : NO
verilog2001 : YES
Optimize Instantiated Primitives : NO
tristate2logic : Yes

3) Translate

The default settings are used

4) Map. NOTE: Items in **RED** are different from the default values

Design Information

Command Line : map -p xc2v500-fg456-5 **-ol med** -timing -cm area -pr b -k 4 -c 100 -tx off -o top_map.ncd top.ngd top.pcf

Target Device : x2v500
Target Package : fg456
Target Speed : -5
Mapper Version : virtex2 -- $Revision: 1.16.8.1 $

5) Place and Route

   par -w **-ol high** -t 1 top_map.ncd top.ncd top.pcf

6) Bit File Generation

   The default settings are used

ISE Settings for QT32b Projects

1) The part number is xc3s400-4pq208
2) Synthesis: NOTE: 6 Items in **RED** are different from the default values

```
=========================================================================
*                    Synthesis Options Summary                          *
=========================================================================
---- Source Parameters
Input File Name                    : top_pads.prj
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO
Verilog Include Directory          :

---- Target Parameters
Output File Name                   : top_pads
Output Format                      : NGC
Target Device                      : xc3s400-4-pq208

---- Source Options
Top Module Name                    : top_pads
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
FSM Style                          : lut
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
ROM Style                          : Auto
Mux Extraction                     : YES
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : YES
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
Resource Sharing                   : YES
Multiplier Style                   : auto
Automatic Register Balancing       : No
```

---- Target Options
Add IO Buffers : NO
Global Maximum Fanout : 65535
Add Generic Clock Buffer(BUFG) : 8
Register Duplication : YES
Equivalent register Removal : NO
Slice Packing : YES
Pack IO Registers into IOBs : auto

---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Keep Hierarchy : SOFT
Global Optimization : AllClockNets
RTL Output : Yes
Write Timing Constraints : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : upper
Slice Utilization Ratio : 100
Slice Utilization Ratio Delta : 5

---- Other Options
lso : top_pads.lso
Read Cores : YES
cross_clock_analysis : NO
verilog2001 : YES
Optimize Instantiated Primitives : NO

3) Translate

The default settings are used

4) Map

Design Information

Command Line : C:/Xilinx62i/bin/nt/map.exe -intstyle ise -p xc3s400-pq208-4 -ol med -timing -cm area -pr b -k 4 -c 100 -tx off -o top_pads_map.ncd top_pads.ngd top_pads.pcf
Target Device : x3s400
Target Package : pq208
Target Speed : -4
Mapper Version : spartan3 -- $Revision: 1.16.8.1 $

5) Place and Route

par -w -intstyle ise -ol high -t 1 top_pads_map.ncd top_pads.ncd top_pads.pcf

6) Bit File Generation

The default settings are used

Generating the Combined MCS File

The final mcs file is generated using iMPACT.

1) Copy the cdf file from another project to the current project directory.
2) Edit the cdf file using any text editor (it is an ASCII file) so that the ConfigDataPath, Collection and both Device Files point to the correct values. Lines shown in RED below are the ones that need to be changed:

```
JedecChain;
FileRevision(JESDxxA);
/* ExpertMode */
/* Active Mode PFF */
/* Mode BS */
/* Cable parallel lpt1 */
/* Mode SS */
/* Mode SM */
/* Mode BSFILE */
/* Mode HW140 */
/* Supermode FileMode */
/* ConfigDevice PFF "xcf08p" 0 0 */
/* PromDevice "xcf08p" 1048576 */
/* Revision */
/* ConfigDevicePath ("C:\Users\egj-work\Documents\FPGA\Star\QT\qt32b_l0_v7_6/") */
/* Format mcs */
/* FillValue FF */
/* BitSwap FALSE */
/* LoadDirection UP */
/* Collection "qt32b_l0_v7_6" */
/* Version 0 "0" */
/* ConcurrentChain 0 */
 P ActionCode(Cfg)
  Device
   PartName(xc3s400)
   File("C:\Users\egj-work\Documents\FPGA\Star\QT\qt32b_l0_v7_6\top_pads.bit")
  ;
 P ActionCode(Cfg)
  Device
   PartName(xc2v500)
   File("C:\Users\egj-work\Documents\FPGA\Star\QT\qt8b_v7_6\top.bit")
  ;
ChainEnd;
```

3) Launch iMPACT and click “Cancel” in any window that pops up to ask what you want to do.
4) When you get to the main iMPACT window click on “Open” in the “File” pull-down menu. Select the new cdf file and click OK. There will be messages in the log window, and then in the main window you should see “Generation Successful”.