QT Address Space Breakdown:

Bits	31…28	27…24	23…20	19…16	15…12	11…8	7…4	3...0
DATA	YYYY	YYYY	0CCC	CCAA	AAAA	AAAA	AAAA	AAAA
LUT	YYYY	YYYY	1CCC	CC00	00AA	AAAA	AAAA	AAAA
Daughter Registers	YYYY	YYYY	1BB1	1100	0100	0000	RRRR	RRRR
Slew Correction Registers	YYYY	YYYY	1BB1	1100	0101	0000	RRRR	RRRR
Mother Registers	YYYY	YYYY	1000	0000	0100	0001	RRRR	RRRR

Y = board address B = daughter number C = channel number
A = data/LUT address R = register address

QT Memory Map:

Memory Block	**Starting Address**	**Ending Address**	**Number of Addresses**	**Data Mask (i.e. valid bits)**
Data Memory Daughter 1	0xYY000000	0xYY1fffff	0x80000 = 2^{21}	0xffffffff
Data Memory Daughter 2	0xYY200000	0xYY3fffff	0x80000 = 2^{21}	0xffffffff
Data Memory Daughter 3	0xYY400000	0xYY5fffff	0x80000 = 2^{21}	0xffffffff
Data Memory Daughter 4	0xYY600000	0xYY7fffff	0x80000 = 2^{21}	0xffffffff
LUT 1	0xYY800000	0xYY803fff	0x1000 = 2^{12}	0x00000fff
LUT 2	0xYY840000	0xYY843fff	0x1000 = 2^{12}	0x00000fff
LUT 3	0xYY880000	0xYY883fff	0x1000 = 2^{12}	0x00000fff
LUT 4	0xYY8c0000	0xYY8c3fff	0x1000 = 2^{12}	0x00000fff
LUT 5	0xYY900000	0xYY903fff	0x1000 = 2^{12}	0x00000fff
LUT 6	0xYY940000	0xYY943fff	0x1000 = 2^{12}	0x00000fff
LUT 7	0xYY980000	0xYY983fff	0x1000 = 2^{12}	0x00000fff
LUT 8	0xYY9c0000	0xYY9c3fff	0x1000 = 2^{12}	0x00000fff
Daughter 1 Registers	0xYY9c4000	0xYY9c40ff	0x100 = 64	0xffffffff
Daughter 1 Slew Correction Regs	0xYY9c5000	0xYY9c50ff	0x100 = 64	0xfff
LUT 9	0xYYa00000	0xYYa03fff	0x1000 = 2^{12}	0x00000fff
LUT 10	0xYYa40000	0xYYa43fff	0x1000 = 2^{12}	0x00000fff
LUT 11	0xYYa80000	0xYYa83fff	0x1000 = 2^{12}	0x00000fff
LUT 12	0xYYac0000	0xYYac3fff	0x1000 = 2^{12}	0x00000fff
LUT 13	0xYYb00000	0xYYb03fff	0x1000 = 2^{12}	0x00000fff
LUT 14	0xYYb40000	0xYYb43fff	0x1000 = 2^{12}	0x00000fff
LUT 15	0xYYb80000	0xYYb83fff	0x1000 = 2^{12}	0x00000fff
LUT 16	0xYYbc0000	0xYYbc3fff	0x1000 = 2^{12}	0x00000fff
Daughter 2 Registers	0xYYbc4000	0xYYbc40ff	0x100 = 64	0xffffffff
Daughter 2 Slew Correction Regs	0xYYbc5000	0xYYbc50ff	0x100 = 64	0xfff
LUT 17	0xYYc00000	0xYYc03fff	0x1000 = 2^{12}	0x00000fff
LUT 18	0xYYc40000	0xYYc43fff	0x1000 = 2^{12}	0x00000fff
LUT 19	0xYYc80000	0xYYc83fff	0x1000 = 2^{12}	0x00000fff
LUT 20	0xYYcc0000	0xYYcc3fff	0x1000 = 2^{12}	0x00000fff
LUT 21	0xYYd00000	0xYYd03fff	0x1000 = 2^{12}	0x00000fff
LUT 22	0xYYd40000	0xYYd43fff	0x1000 = 2^{12}	0x00000fff
LUT 23	0xYYd80000	0xYYd83fff	0x1000 = 2^{12}	0x00000fff
LUT 24	0xYYdc0000	0xYYdc3fff	0x1000 = 2^{12}	0x00000fff
Daughter 3 Registers	0xYYdc4000	0xYYdc40ff	0x100 = 64	0xffffffff
Daughter 3 Slew Correction Regs	0xYYdc5000	0xYYdc50ff	0x100 = 64	0xfff
LUT 25	0xYYe00000	0xYYe03fff	0x1000 = 2^{12}	0x00000fff
LUT 26	0xYYe40000	0xYYe43fff	0x1000 = 2^{12}	0x00000fff
LUT 27	0xYYe80000	0xYYe83fff	0x1000 = 2^{12}	0x00000fff
LUT 28	0xYYec0000	0xYYec3fff	0x1000 = 2^{12}	0x00000fff
LUT 29	0xYYf00000	0xYYf03fff	0x1000 = 2^{12}	0x00000fff
LUT 30	0xYYf40000	0xYYf43fff	0x1000 = 2^{12}	0x00000fff
LUT 31	0xYYf80000	0xYYf83fff	0x1000 = 2^{12}	0x00000fff
LUT 32	0xYYfc0000	0xYYfc3fff	0x1000 = 2^{12}	0x00000fff
Daughter 4 Registers	0xYYfc4000	0xYYfc40ff	0x100 = 64	0xffffffff
Daughter 4 Slew Correction Regs	0xYYfc5000	0xYYfc50ff	0x100 = 64	0xfff
Mother Registers	0xYY804100	0xYY8041ff	0x100 = 64	0xffffffff

Mother Registers:

ID: Name	Address	Functionality	Access
0: Mother ID	0xYY804100	This register returns : 0xabcdMMmm for QT32b 0xfedcMMmm for QT32c where : MM = major version number of QT32 code mm = minor version number of QT32 code	Read Only
1: Gate Start Delay	0xYY804104	D0-D7: Delay for gate start signal. Steps of 1 ns. Range of 255 ns. (8 bits). Use this to move Gate Reset with respect to RHIC Clock.	Read/Write
2: Output Latch Delay	0xYY804108	D0-D7: Delay of output from QT board to DSMI. Steps of 1ns. Range of 255ns.	Read/Write
3: Discriminator Threshold	0xYY80410c	D0-D9: One threshold per board. The translation from register value to mV is different for each combination of board types: QT32b + any DC: Reg in decimal = 2*(Th in mV) – 1.8 QT32c + v1.3 DC: Reg in decimal = 4*(Th in mV) + 16 QT32c + v1.5 DC: Reg in decimal = 2*(Th in mV) – 1.4	Read/Write
4: Vp	0xYY804110	D0-D9: Test pulse height. One per board.	Read/Write
5: Run Mode Settings	0xYY804114	D0: RCC/Local Oscillator Mode 0 = RCC Mode 1 = Local Oscillator Mode	Read/Write
6: Prom Programming 1	0xYY804118	D0-D31: Prom Programming Status	Read Only
7: Prom Programming 2	0xYY80411c	D0-D7: TDI bit stream length	Write Only
8: Prom Programming 3	0xYY804120	D0-D31: Prom Programming bitstream data in	Write Only
9: Prom Programming 4	0xYY804124	D0-D31: Prom Programming Readback	Read Only
10: Even/Odd Pulse Injection	0xYY804128	D0: Single Even Channel Pulse (1 RS) D1: Single Odd Channel Pulse (1 RS) (Even/Odd based on channels numbered 1 to 8)	Read/Write
11: Status	0xYY80412c	D0: DAC Busy – After writing to a DAC register (gate_start, gate_stop, output_latch_delay, disc_thresh, Vp), you must wait until this bit is clear. D1-D31 : Undefined	Read Only
12: Reserved	0xYY804130	Reserved	
13: Zero Suppression Mode	0xYY804134	D0: Use zero suppression when reading out board. All daughter data is still read by mother but data is zero suppressed when read over VME.	Read/Write
14: DCM Reset	0xYY804138	D0: Manually reset motherboard DCM.	Read/Write
15: Gate End Delay	0xYY80413c	D0-D7: Delay for gate end signal. Steps of 1 ns. Range of 255ns.	Read/Write
16: Serial Number Lo	0xYY804140	D0-D31: Lower 32 bits of serial number. Writing a 1 to bit 0 will cause the board to reread its serial number.	Read/Write
17: Serial Number Hi	0xYY804144	D0-D31: Upper 32 bits of serial number.	Read Only
18: Read Data Offset	0xYY804148	D0-D15: Writing offset starts motherboard reading data for each channel at specified memory offset. (There are 0xffff possible memory slots for each channel)	Read/Write
19: Data Read Status	0xYY80414c	D0: 1 = Motherboard busy reading daughter data 0 = Daughter data ready to read	Read Only
20: Number Data Words	0xYY804150	D0-D5: Number of data words available to read(0–32)	Read Only
21: Data Word [0]	0xYY804154	D0-D31: 1st data word	Read Only
22: Data Word [1]	0xYY804158	D0-D31: 2nd data word	Read Only
…	…		
52: Data Word [31]	0xYY8041D0	D0-D31: 32nd data word	Read Only
53: Even Pulse Prescale	0xYY8041D4	D0-D31: Continuous Even Channel Pulse – 1 RS in length, prescaled by this value. (Even/Odd based on channels numbered 1 to 8) (Prescale > 1000 to get max ADC values)	Read/Write
54: Odd Pulse Prescale	0xYY8041D8	D0-D31: Continuous Odd Channel Pulse – 1 RS in length, prescaled by this value. (Even/Odd based on channels numbered 1 to 8) (Prescale > 1000 to get max ADC values)	Read/Write
55: DAC/Delayline Status	0xYY8041DC	D0-D31: DAC/Delayline state machine status	Read Only
56: TAC Stop Delay (QT32C ONLY)	0xYY8041E0	QT32C Register ONLY : D0-D7: TAC Stop Delay. ½ ns steps for a range of 128 ns	Read/Write
57: TAC Stop Busy (QT32C ONLY)	0xYY8041E4	QT32C Register ONLY : D0: DAC Busy – After writing the TAC Stop register you must wait until this bit is clear.	Read Only

58: TAC Stop Status (QT32C ONLY)	0xYY8041E8	QT32C Register ONLY : D0-D31: TAC Stop state machine status	Read Only
99: Local Oscillator Mode	0xYY804014	D0: Run/Stop_n when obeying local oscillator mode.	Read/Write

Daughter Registers (1 set per daughter) (Z = 9,B,D,F):

ID: Name	Address	Functionality	Access
0: Daughter ID	0xYYZc4000	This register returns 0xabcdN0XY where: N = geo ID (0,1,2 or 3) X = major version number of QT8 algorithm Y = minor version number of QT8 algorithm	Read/Write
1: Compilation Date/Version	0xYYZc4004	This register returns 0xYYMMDDVV where: YYMMDD = date when daughter code is compiled VV = version number on that date	Read Only
2: Data Start Address	0xYYZc4008	D0-15: Address to start writing data to when entering run mode. One per daughter.	Read/Write
3: Use LUT	0xYYZc400c	D0: Route input data through the LUT before storing to memory. If disabled, route input data directly to memory. One per daughter. NOTE: Data to L0 always goes through the LUT regardless of this setting.	Read/Write
4: Clear SRAM	0xYYZc4010	D0: Initiate “clear memory” cycles for the SRAM	Write
5: Clear SRAM BUSY	0xYYZc4014	D0: ‘1’ when “clear memory” cycle is in progress and ‘0’ when it is finished.	Read
6: Serial Number Lo	0xYYZc4018	D0-D31: Lower 32 bits of serial number. Writing a 1 to bit 0 will cause the board to reread its serial number.	Read/Write
7: Serial Number Hi	0xYYZc401c	D0: Upper 32 bits of serial number.	Read Only
8: Reserved	0xYYZc4020	Reserved	
9: Clk Status and Reset	0xYYZc4024	D0: ADC LVDS Clk DCM Locked (from ADC) D1: Sysclk DCM Locked (from motherboard) D2: ADC Clk DCM 1 Locked (to ADC) D3: ADC Clk DCM 2 Locked (to ADC) Write a ‘1’ to bit 0 to reset all DCMs	Read/Write
10: Algorithm Latch Offset	0xYYZc4028	D0-D2: Set timing of algorithm output latch: 0 = unclocked algorithm output 1 – 7 = delayed algorithm latches (increments ~14ns) D8-D10: Set timing of direct-to-L0 output latch: 0 = unclocked direct-data output 1 – 7 = delayed direct-data latches (increments ~14ns NOTE: Using the direct-to-L0 output path requires special versions of the Daughter and Mother (L0 FPGA) code, which have only ever been implemented in algorithm 6.f for the ZDC.	Read/Write
11: Trigger Mask	0xYYZc402c	D0-D15: Mask channels from trigger but not data. 0 = unmasked (default for all channels) 1 = masked D0 = channel 0, etc (v5_8 – bits D0-D7 mask bits from HT trigger bits D8-D15 mask bits from Sum trigger other versions–bits D0-D7 mask ALL data from trigger bits D8-D15 are unused)	Read/Write
12: Output Ramps	0xYYZc4030	D0-D3: Unused D4: Output ramps to L0 after memory (outmem) D5: Output ramps to L0 before memory (inmem)	Read/Write
13: Algorithm Register 0	0xYYZc4034	D0-D11: ADC Threshold for “good hit” v5_2, v5_3, v5_4 – applied to channels 0-3	Read/Write
14: Algorithm Register 1	0xYYZc4038	D0-D11: TAC Min for “good hit” v5_2, v5_3, v5_4 – applied to channels 4-7	Read/Write
15: Algorithm Register 2	0xYYZc403c	D0-D11: TAC Max for “good hit” v5_2, v5_3, v5_4 – applied to channels 4-7	Read/Write
16: Algorithm Register 3	0xYYZc4040	See Algorithm Document	Read/Write
17: Algorithm Register 4	0xYYZc4044	See Algorithm Document	Read/Write
18: Algorithm Register 5	0xYYZc4048	See Algorithm Document	Read/Write
19: Algorithm Register 6	0xYYZc404c	See Algorithm Document	Read/Write
20: Algorithm Register 7	0xYYZc4050	See Algorithm Document	Read/Write
21: Algorithm Register 8	0xYYZc4054	See Algorithm Document	Read/Write

Additional Daughter Registers (1 set per daughter) (Z = 9,B,D,F)

ID: Name	Address	Functionality	Access
22: Algorithm Register 9 (QT8B) TAC Gain Control (QT8-TAC)	0xYYZc4058	QT8B Register: See Algorithm Document QT8-TAC Register: D0-D11 : 12 bits of DAC Data D13-D15 : DAC Address : 000 = TAC Channels 001 = Monitor Channels D16 : 0 = Write, 1 = Read (Read is not implemented) D17-D18 : DAC Channel (values 0-3)	QT8B Read/Write QT8-TAC Write Only
23: Algorithm Register 10	0xYYZc405c	See Algorithm Document	Read/Write
24: Algorithm Register 11	0xYYZc4060	See Algorithm Document	Read/Write
25: Algorithm Register 12	0xYYZc4064	See Algorithm Document	Read/Write

Slew Correction Registers (1 set per daughter) (Z = 9,B,D,F):

ID:	Address	Functionality	Access
0	0xYYZc5000	Channel 0 ADC Bin Limit 0	Read/Write
1	0xYYZc5004	Channel 4 TAC Slew Correction Offset 0	Read/Write
2	0xYYZc5008	Channel 1 ADC Bin Limit 0	Read/Write
3	0xYYZc500c	Channel 5 TAC Slew Correction Offset 0	Read/Write
4	0xYYZc5010	Channel 2 ADC Bin Limit 0	Read/Write
5	0xYYZc5014	Channel 6 TAC Slew Correction Offset 0	Read/Write
6	0xYYZc5018	Channel 3 ADC Bin Limit 0	Read/Write
7	0xYYZc501c	Channel 7 TAC Slew Correction Offset 0	Read/Write
8	0xYYZc5020	Channel 0 ADC Bin Limit 1	Read/Write
9	0xYYZc5024	Channel 4 TAC Slew Correction Offset 1	Read/Write
10	0xYYZc5028	Channel 1 ADC Bin Limit 1	Read/Write
11	0xYYZc502c	Channel 5 TAC Slew Correction Offset 1	Read/Write
12	0xYYZc5030	Channel 2 ADC Bin Limit 1	Read/Write
13	0xYYZc5034	Channel 6 TAC Slew Correction Offset 1	Read/Write
14	0xYYZc5038	Channel 3 ADC Bin Limit 1	Read/Write
15	0xYYZc503c	Channel 7 TAC Slew Correction Offset 1	Read/Write
…	…	…	…
56	0xYYZc50e0	Channel 0 ADC Bin Limit 7	Read/Write
57	0xYYZc50e4	Channel 4 TAC Slew Correction Offset 7	Read/Write
58	0xYYZc50e8	Channel 1 ADC Bin Limit 7	Read/Write
59	0xYYZc50ec	Channel 5 TAC Slew Correction Offset 7	Read/Write
60	0xYYZc50f0	Channel 2 ADC Bin Limit 7	Read/Write
61	0xYYZc50f4	Channel 6 TAC Slew Correction Offset 7	Read/Write
62	0xYYZc50f8	Channel 3 ADC Bin Limit 7	Read/Write
63	0xYYZc50fc	Channel 7 TAC Slew Correction Offset 7	Read/Write