Hardware Description for the STAR Trigger Control Unit – Mark 4

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The 4th version of the STAR TCU consists of 5 connected PC boards as shown here in Figure 1. The DSMI, TCUI and TCUR have not been modified from their original design. However the TCU motherboard has now been modified to support an upgraded TCU daughter card: the TCUD-2.

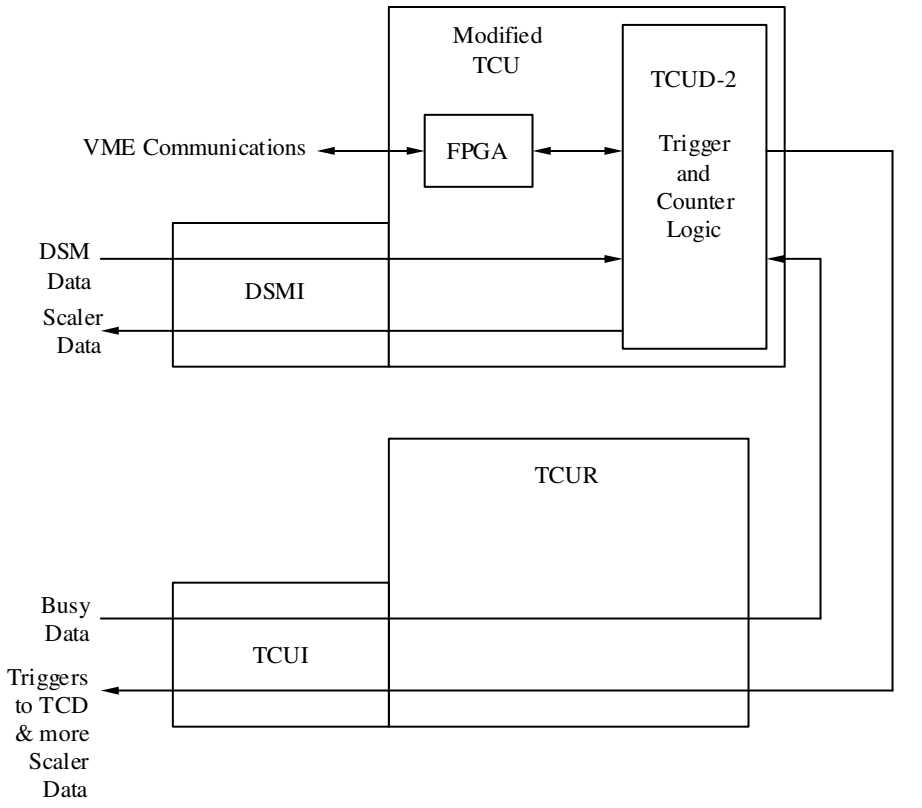


Figure 1: Data Flow through the 5 Sections of the TCU4

All the trigger and counter logic is implemented on the TCUD-2. Data enters from both the DSMI and TCUI/TCUR paths, and is also driven out on both paths. The connection between the TCU motherboard and the TCUR is implemented using two 120-pin front panel cables. Communication is a multi-step process. An FPGA on the motherboard implements the VME Slave protocol so it can communicate with an external VME Master over a backplane. That FPGA also implements a custom, simple, protocol to communicate directly with the TCUD-2. The hardware connections exist to enable the TCUD-2 to communicate with an FPGA on the TCUR. However, the logic to implement this path has not been created yet. The trigger and counter logic in the TCUD-2 is synchronous with the RHIC clock. The communications logic is

synchronous with a local 66 MHz oscillator. The distribution scheme for these two clocks is shown in Figure 2.

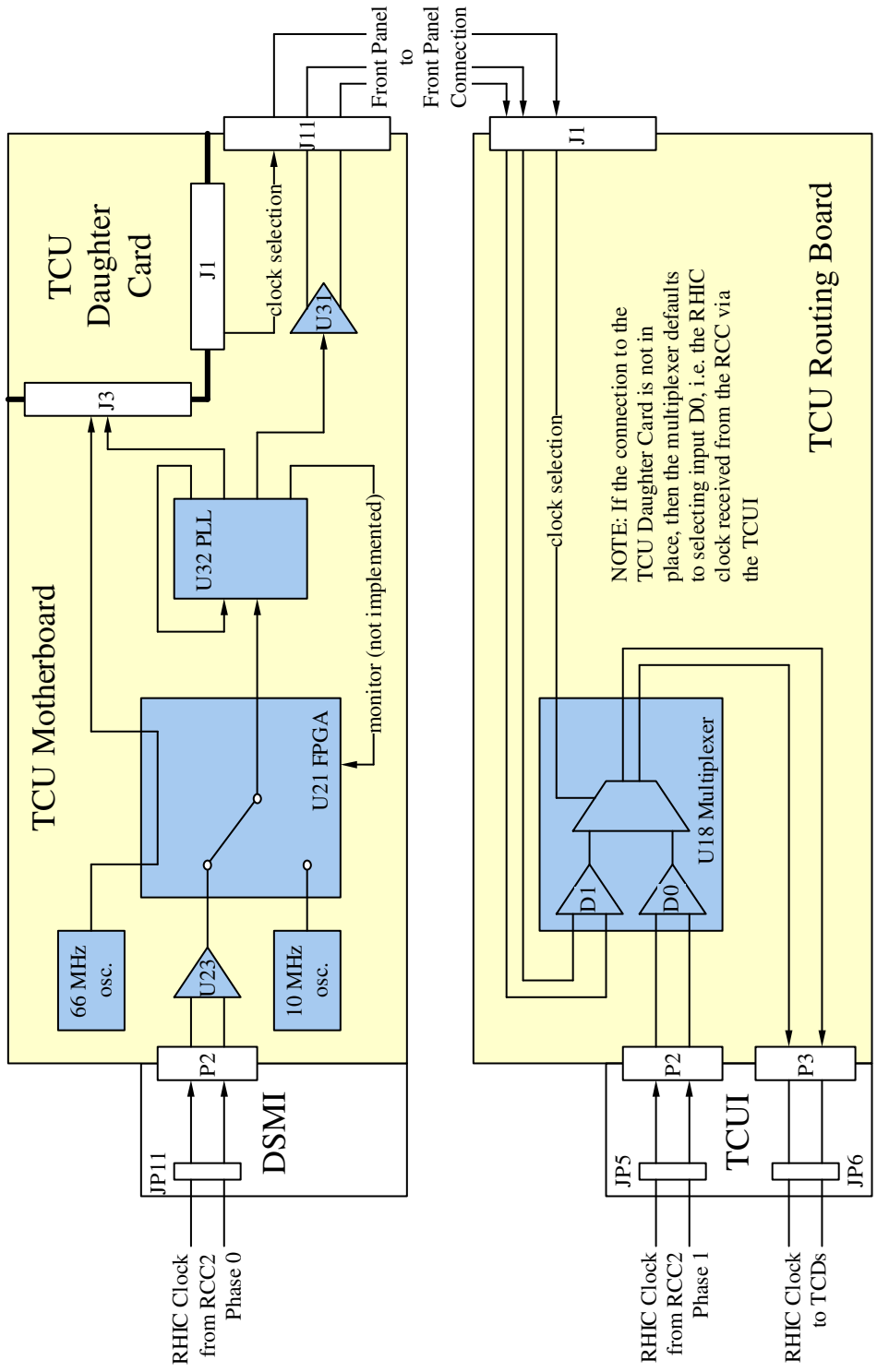


Figure 2: Clock Distribution through the 5 Sections of the TCU4

Modifications to the TCU motherboard were necessary in order to allow it to support the new TCUD-2. Some level shifters had to be reconfigured to allow them to translate between 5V and 2.5V domains, instead of 5V and 3.3V domains. Two banks of pins on the motherboard FPGA also needed to be converted from 3.3V to 2.5V. These patches are shown in Figure 3. This was all necessary because the Virtex-6 FPGA used on the TCUD-2 is not compatible with 3.3V signals.

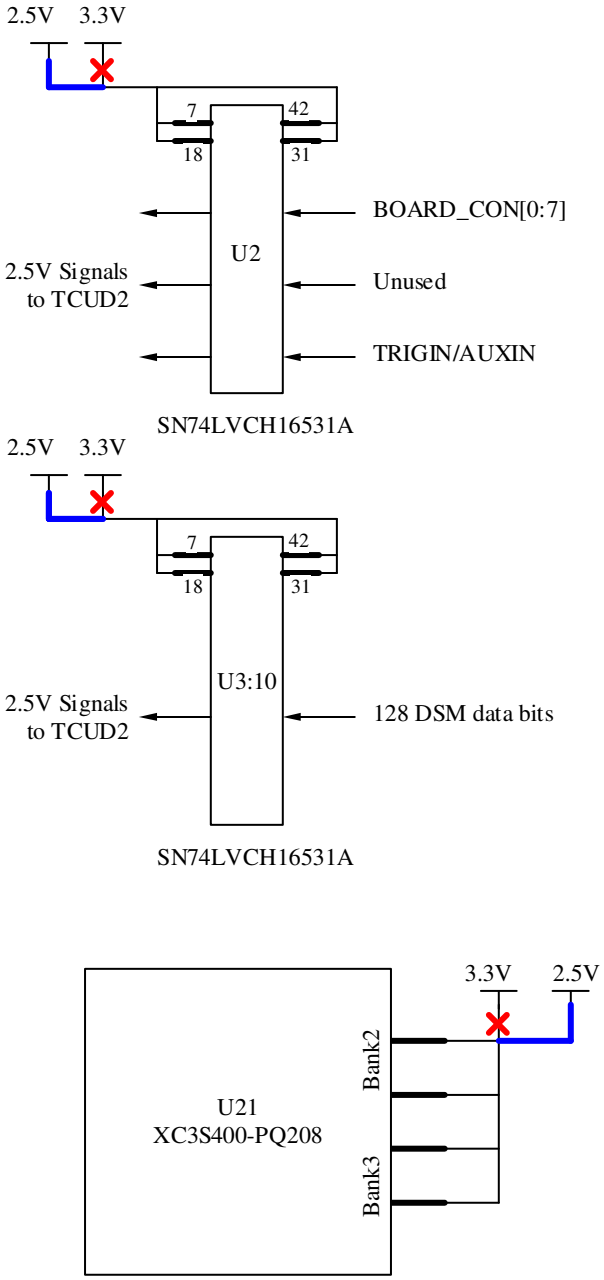


Figure 3: TCU Motherboard Patches

A block diagram of the TCUD-2 itself is shown in Figure 4. It consists primarily of a Xilinx Virtex-6 FPGA and level shifters to convert between 3.3V signals and 2.5V signals.

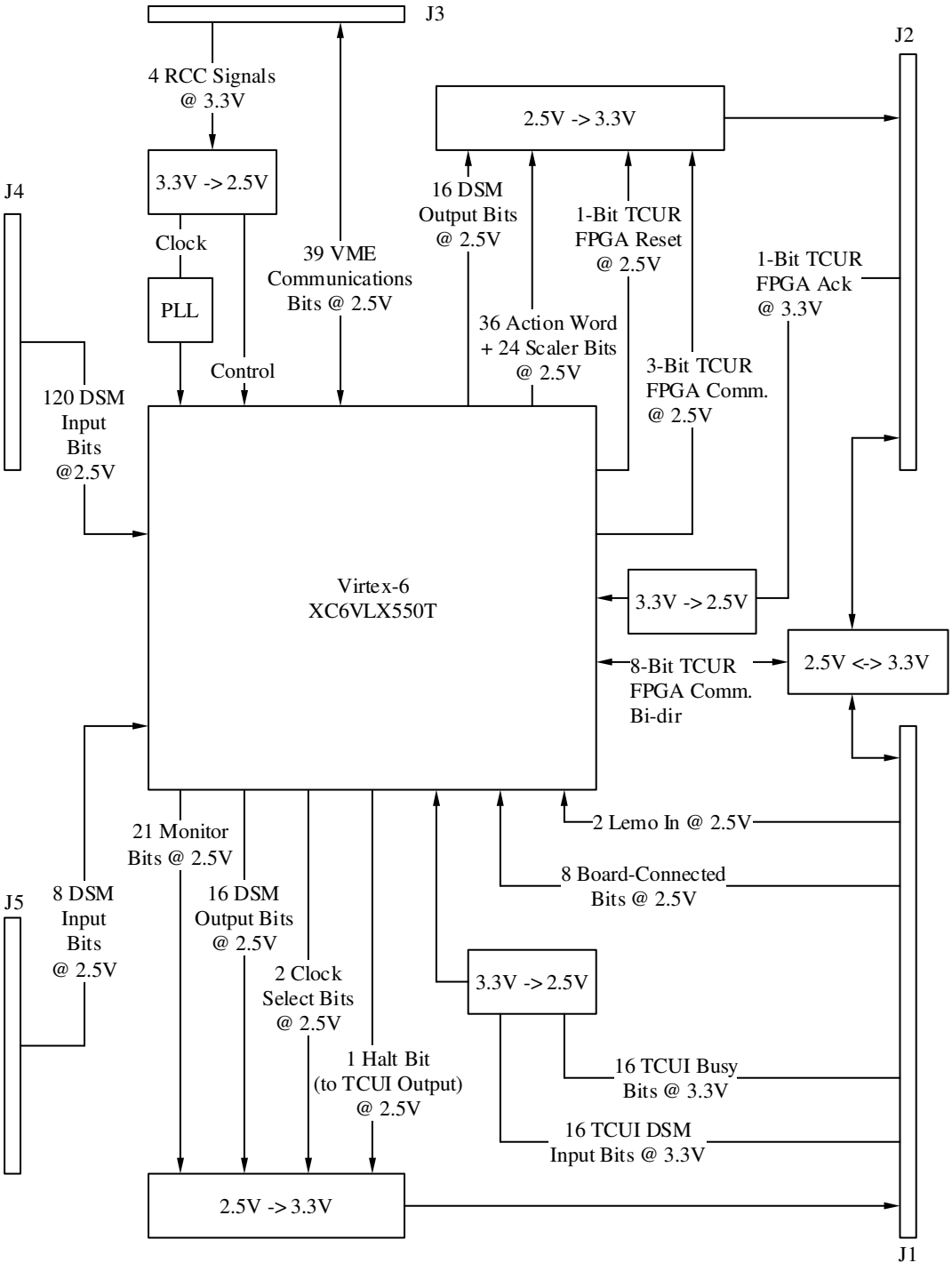


Figure 4: Block Diagram of the 2nd Version of the TCU Daughter Card

Some signals (the 128 DSM input bits and the motherboard communications bits) have already been converted on the motherboard itself so there are no additional level shifters necessary for them here. The PLL is necessary to double the incoming RHIC clock frequency so that it is within the range accepted by the PLL built into the FPGA.

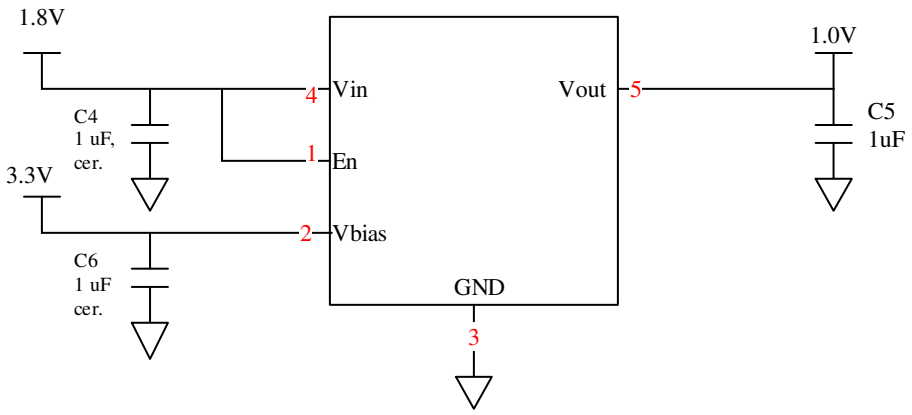
The full list of parts is given below:

Item	Part Number/Footprint	Description	Reference #
1	Socket for Xilinx XC6VLX550T-2FF1760	Socket for FPGA in FF1760 package. Footprint includes the ball grid array itself, plus a keep-out area for the socket and the socket's mounting holes.	U15
2	Micron (Numonyx) PC28F512P30T	512 Mbit Flash Memory	U16
3	BLKCON.100/VH/TM1SQS/W.100/6	Right-angled 6-pin Header	J14
4	SM/D_0805_21	Red Surface Mount LED	D1
5	Size = D7374 = 7.3x4.3x2.9 mm	330 uF Tantalum Capacitors	C64, C65, C66, C67, C68, C69, C70, C71, C72
6	Cypress CY7B9950AXC	Phase-Locked Loop	U4
7	TI SN74AVC32T245ZKER	32-bit Bus Transceiver	U6, U11, U12
8	TI SN74AVC20T245DGVR	20-bit Bus Transceiver	U9, U13
9	TI SN74AVC16T245DGVR	16-bit Bus Transceiver	U8, U10
10	TI SN74AVC8T245 DGVR	8-bit Bus Transceiver	U5
11	TI SN74AVC4T245 DGVR	4-bit Bus Transceiver	U3
12	TI SN74AVC1T45DCKR	1-bit Bus Transceiver	U14
13	Hirose FX11LA-120P/12-SV(71)	Motherboard Connectors	J1, J2, J3, J4, J5
14	Size = 0603	100 nf capacitors	C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C24, C25, C26, C27, C28, C29, C30, C31, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63
15	Micrel MIC37151-1.8WR	Voltage Regulator	U1
16	See patch description on pages 6 & 7	No Load part	U2
17	SM/CT_7343_12	100 uF polarized capacitor	C1
18	Size = 0805	10 uF capacitor	C2

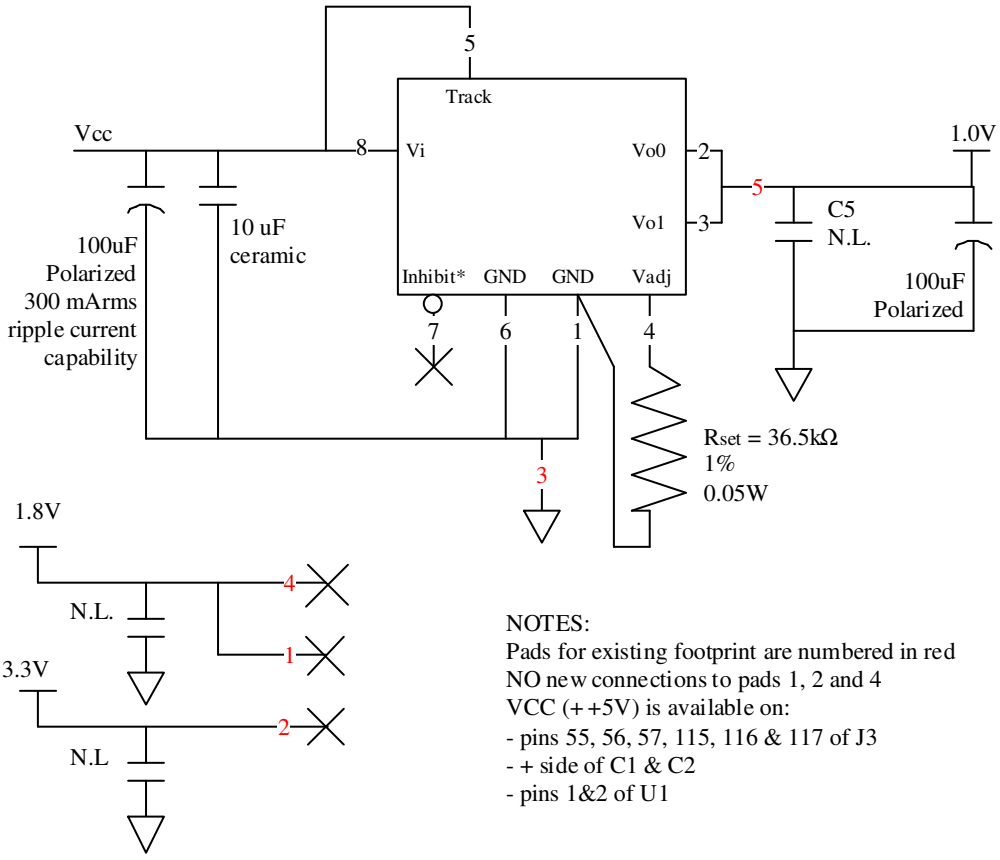
19	Size = 1210	47 uF ceramic polarized capacitor	C3
20	Size = 0805	No Load (NL) capacitor	C4, C5, C6
21	Size = 0603	No Load (NL) resistor	R14, R15
22	Keystone Electronics 5001 (Digikey 5001K-nd)	Single-pin header with plated thru hole of .040 inches or 1.02mm	J6, J7, J8, J9, J10, J11, J12, J13
23	BLKCON.100/VH/TM1SQS/W.100/8	Right-angled 8-pin Header	J15
24	Size = 0603	100K Resistor	R1
25	Size = 0603	0 Ohm resistor	R2, R3
26	Size = 0603	4.7K resistors	R4, R5, R8, R9, R10, R11, R12, R13
27	Size = 0603	1K resistor	R6
28	Size = 0603	330 Ohm resistor	R7
29	TI CDCLVC1102PWR	1:2 Fanout Buffer	U7

Unfortunately a patch was found to be necessary to part U2, the 1.0 V voltage regulator on the TCUD-2. The original regulator was a Micrel MIC49200-1.0 which could not provide enough current. It was replaced with the PTV05010W from Texas Instruments that had to be patched in. The patch is shown in Figure 5.

Existing Connections for U2



New Connections for U2



NOTES:
Pads for existing footprint are numbered in red
NO new connections to pads 1, 2 and 4
VCC (++5V) is available on:
- pins 55, 56, 57, 115, 116 & 117 of J3
- + side of C1 & C2
- pins 1&2 of U1

Figure 5: Voltage Regulator Patch for the TCUD-2