180802

Requirements for QTI2

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This second version of the QT Interface (QTI2) card is a back-of-crate board for use with QTC mother boards. It is intended to replace the TAC boards and the analog NIM circuitry currently in use by QTB boards to feed the hit multiplicity (0 or >0) to the Rhic and RICH scalers from the BBCEast, BBCWest, VPDE, and VPDW. The QTI2 will accept discriminator output from the 16 QTC channels on the P2 backplane behind each mother board. It will have the capability to forward those discriminated signals in PECL format to another device (e.g. RAT board, NIMULET, etc.) via 34 pin IDC connector. Each QT daughter card (DC) will put 6 bits onto P2 - the 4 discriminator bits, an OR of these bits, and a spare. The QTI2 will form an OR of the 4 DC OR bits to send to the Rhic and RICH scalers. Each QTI2 must also pass the 32 bits of the QT algorithm output from P3 to the DSM tree. Each of the BBC and VPD boards services 16 channels of either E or W inputs: a single board can thus provide a hit signal for E and W separately.

Requirement 1: Connect to both J2[1] and J3 A and C rows behind a QTC board in a VME crate.
Justification: Discriminator hits come from the mother board on P2 and algorithm output comes as 32 bits on P3.

Requirement 2: Export the 16 discriminator hit bits via 34 pin IDC male connector (with short profile latches) in PECL format.
Justification: these signals input to the RAT Board and subsequently pass to the Scaler48 system. There the BBC and VPD signals are used for polarimetry and luminosity monitoring.

Requirement 3: put 32 algorith output bits from J3 onto 2 IDC 34 pin connectors for shipment to the DSM tree in PECL standard.
Justification: This is how the DSM tree gets input from the QTC

Requirement 4: provide a NIM output from each board to indicate valid hits>0
Justification: The BBC and VPD both send such hit bits to the luminosity monitors, the Rich and RHIC scalers.
Status: will program the 5th bit of each daughter card to be the Logic OR of its 4 discriminators, calculated in VHDL to allow selection of input bits.
Output is NIM low to indicate a hit.

Note that the current QTI design also includes a 10pin IDC connector to input TAC Stop from an RCC2. While not required, there is no reason to drop this.

[1] P2 is the connector facing the front of the crate; J2 is its mate in the back of the crate.