STAR Trigger Level-0 Upgrade
Requirements for the DSM2 Board

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August 31, 2020

Introduction

The STAR Trigger System performs a quick analysis of data from the fast trigger detectors in order to decide if the slower readout of data from the rest of STAR should be initiated. The current STAR Trigger Level-0 data processing system is based on the Data Storage and Manipulation boards (DSM) and the Charge-Time (QT) digitizer boards. Both boards run synchronously with the RHIC clock, receiving new data from trigger detectors every tick of the clock, processing it and passing on the results. Many QT and DSM boards are linked together to form a tree structure that funnels the results of the data analysis to the Trigger Control Unit (TCU). The TCU then makes the actual trigger decision.

The DSM boards are currently the oldest part of the STAR Trigger system and a number of problems have appeared. This document describes those problems, and then specifies the requirements for a new board that will solve those problems and also enable future upgrades.

Problems with the existing DSM System

The existing DSM system met all of the original requirements when it was first installed. However, over the years the system has grown, the needs of the users have evolved and now several problems have arisen.

- The electronics is so old that replacement parts are no longer available
- The existing DSM boards are read out in series within each crate over the VME backplane under the control of a VME CPU. This relatively slow readout mechanism is now limiting the overall STAR trigger rate.
- The boards are also configured (in series) and monitored from that same VME CPU using the same VME backplane. Using that VME infrastructure for all of these purposes increases the time taken to configure the system and limits the extent to which the boards can be monitored.
- Over time the users' trigger requirements have grown to include more complex trigger algorithms. The processing unit (FPGA) on the existing DSM boards does not have the capability to implement the most complex algorithms.
- Data I/O on the current DSM is limited to relatively low-speed parallel bit streams with 128 input bits and just 32 output bits. The limited number of output bits from each DSM board, and the fixed structure of the DSM tree place serious limits on the type of data analysis that can be performed at Level-0. For example, an algorithm in which hits in each MTD tray are compared to the ADC sum from the EMC towers with which it overlaps would be really useful. This comparison would make it possible to confirm or exclude the presence of muons, and would therefore make muon triggers much more efficient. Currently the EMC and MTD data are not brought together in the DSM tree

until the end, by which time only summary data is available. Fixing this in the existing system would involve re-cabling the DSM tree, and sacrificing other important connections.

New DSM Board Definition

It is now time to upgrade the DSM system and replace the existing hardware to solve these problems. The most urgent problems are the obsolescence of the existing hardware and the relatively slow readout rate. Those problems have to be solved in order for STAR to take data efficiently at a high rate when RHIC returns to full-energy running. The goal is for the Trigger system to be able to maintain a steady-state event rate of at least 20 kHz.

First, the existing DSM boards will be replaced, one-for-one, with modern boards that include a dedicated high-speed readout path and a separate communications/monitoring path as well as all the existing parallel data I/O connections. The new boards will not include any VME communications capability. Much of the existing functionality, which was implemented in discreet ICs on the PC board, will now be integrated into the FPGA logic. This will result is a significant simplification of the PC board design and also make it possible to multiplex larger data sets onto the existing parallel I/O connections. In addition the board will include a few sockets for pluggable high-speed fiber-optic transceivers. This board will be referred to as DSM2.

Pending latency test results, the firmware in the DSM2 boards might be modified to allow them to send and receive serialized data streams using those transceivers in addition to the existing parallel I/O. More complex algorithms could then be implemented in the DSM2 boards that received both serial and parallel input data.

This development is shown in Figures 1 and 2. Figure 1 shows a block diagram of the existing DSM board and figure 2 shows DSM2.

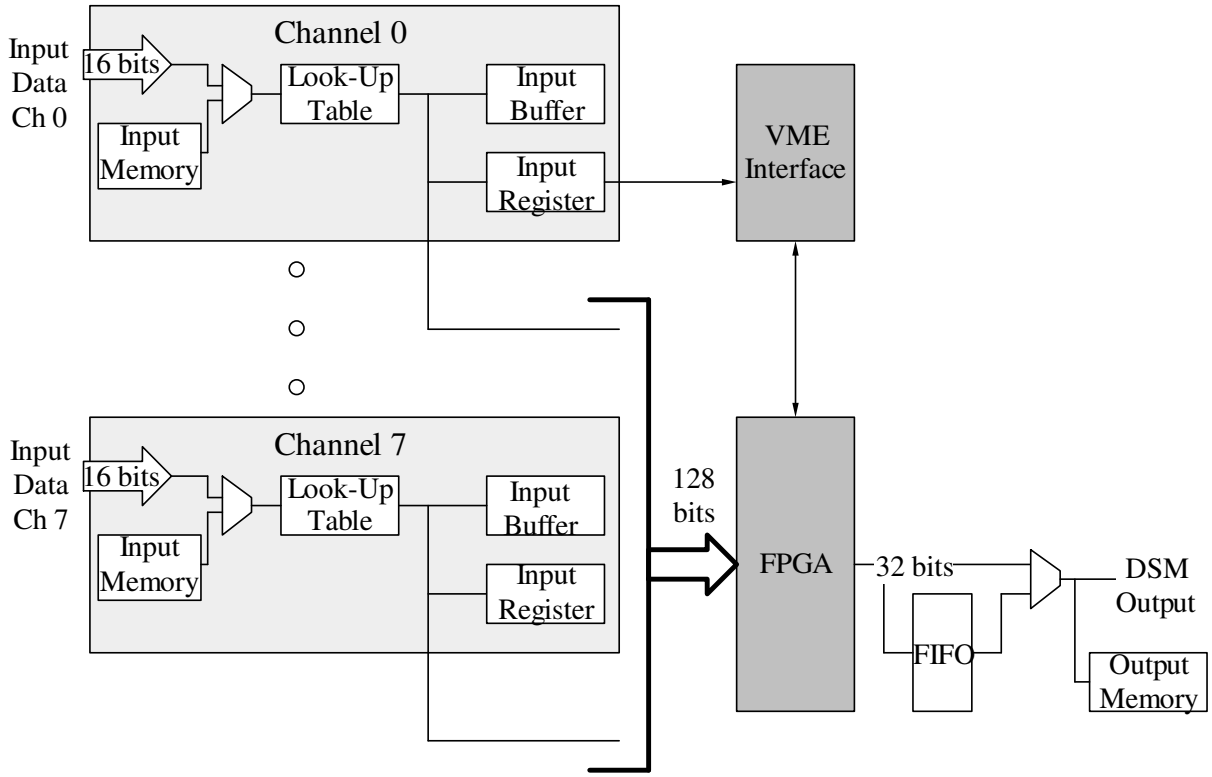

Figure 1: The original DSM board

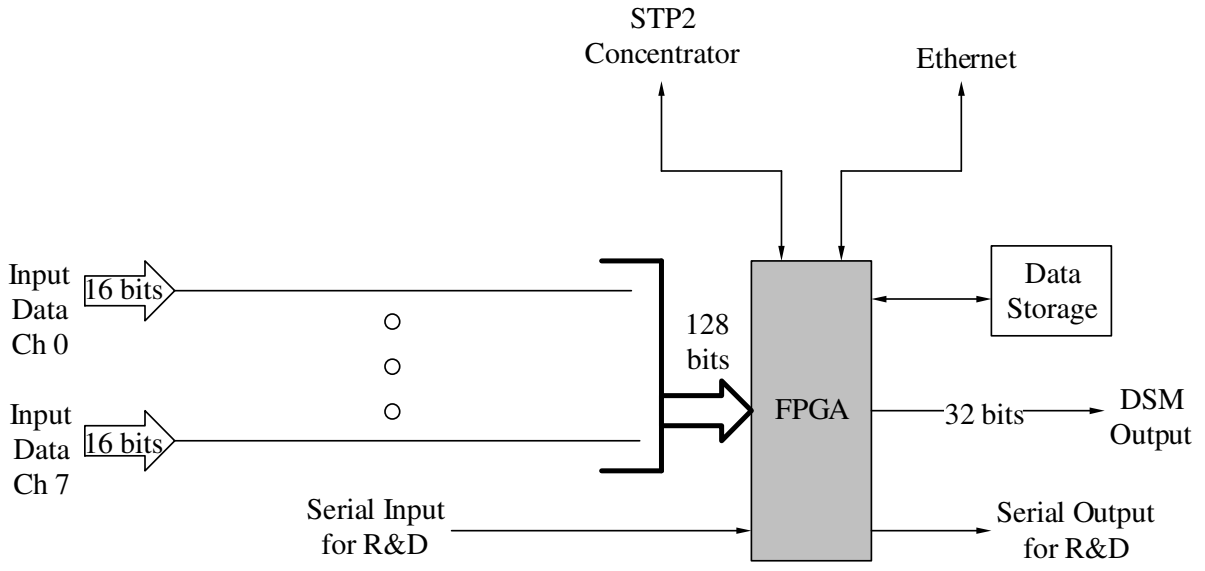

Figure 2: DSM2, which includes all the original parallel I/O connections as well as a connection to the fast STAR Trigger Pusher (STP2) network and serial I/O connections for future use.

DSM2 Board Requirements

Hardware

1) Requirement: **Form Factor**. The DSM2 Board needs to have the extended 9U VME Form Factor. "Extended" means the board should measure 400 mm from front panel to back-plane, which is longer than the standard VME size-D length of 340 mm.
   Justification: These boards need to plug into the existing VME crates and connect to the existing DSMI/TDSMI/TofDSMI boards.
   Status: The first prototype board has the wrong form factor. It uses the standard VME size-D form factor (9U x 340 mm) instead of the extended form factor. The next version will have the correct form factor.
2) Requirement: **Power**. The DSM2 Board must use the VME +5V power lines as its power supply.
   Justification: The board must plug into existing VME crates so it makes sense to use those crates as power supplies.
   Status: Tested and working. NOTE: DSM2 also has a barrel power connector that can accept 5V from an external supply for standalone tests.
3) Requirement: **Backplane Daisy-Chains**. The DSM2 must pass through the daisy-chain signals for VME communications (IACK and BG) and the STAR Trigger chain-block transfer.
   Justification: Even though DSM2 will not use either the VME communications path or the STAR Trigger chain-block transfer functionality it will be used in VME crates with other modules that do use those functions. It must not disrupt those functions.
   Status: The first prototype correctly passes through the VME daisy-chain signals (IACK and BG) but not the STAR Trigger chain-block transfer signals. The next version will fix that.
4) Requirement: **Input from VME P3 Connector**. The DSM2 must receive 128 5V TTL bits in parallel through the P3 backplane
   Justification: This is how the existing DSMI/TDSMI/TofDSMI boards present their data.
   Status: Tested and working (see NOTE in Requirement 6 for details of rate tests).
5) Requirement: **Output to VME P2 Connector**. The DSM2 must drive 32 5V TTL bits in parallel through the P2 backplane
   Justification: These bits are used by the existing DSM boards to send data to the next layer of the DSM tree and also to the Scaler System.
   Status: Tested and working (see NOTE in Requirement 6 for details of rate tests).
6) Requirement: **VME I/O Data Routing**. All TTL data bits must connect directly between the VME connectors and the FPGA, i.e. there must be no intermediate circuitry with built-in assumptions about the data timing or the board's running status.
   Justification: This will make it possible to ensure the output is in a deterministic state (i.e. not floating) at all times and potentially to multiplex extra data onto each channel by using a faster clock. The outputs of the existing DSM boards do float when the boards are not running, which has caused problems for downstream subsystems (e.g. the Scalar System). Also, data is latched onto each DSM board on the rising edge of the RHIC clock. The source of this RHIC clock is the primary clock distribution network

on the DSM board, which is independent of the FPGA. As a result it is impossible to change the frequency of the input latch without affecting the rest of the board. This meant it was impossible to accommodate a user who wanted to multiplex extra data onto one channel by using a faster clock.
Status: Tested and working. NOTE: DSM2 has just voltage level-adapters (3.3V <-> 5V) in between the VME backplane connectors and the FPGA. Low statistics loopback tests have been performed at 50 MHz, i.e. approximately 5 times faster than the RHIC clock rate. In these tests the 32 output bits are routed from the FPGA through the VME backplane and back to the FPGA inputs via the DSMI and a pair of Trigger-standard 34-pin Twist-and-Flat cables. The received data is then compared to the transmitted data and differences are flagged as errors. The tests were error-free, demonstrating that it is possible to multiplex larger data sets onto the existing parallel I/O connections.

7) Requirement: **Clock/Control from VME P2 Connector**. The DSM2 must receive the RHIC clock and synchronous control signals through P2 as 5V PECL
Justification: This is how the existing DSMI/TDSMI/Tof-DSMI boards present their clock and control signals.
Status: Tested and working.
8) Requirement: **Local Clock**. The DSM2 must have a local oscillator that can be used instead of the RHIC clock received through the P2 backplane.
Justification: This is necessary for standalone testing.
Status: Tested and working. DSM2 has a 10 MHz on-board oscillator that connects directly to the FPGA.
9) Requirement: **Ethernet Connection**. The DSM2 must include an Ethernet connection.
Justification: A communications path is needed for remote control and monitoring of the board. That path must be separate from the fast readout path. The STAR Trigger Group has been moving away from VME and has standardized on Ethernet for all recent electronics development
Status: Tested and working. DSM2 has the same ConnectCore ™ 9P 9215 module from Digi that is used on the upgraded RHIC Clock and Control module (RCC2), the STP2R and the STP2C boards.
10) Requirement: **STP2 Transceiver.** The DSM2 must include an Enhanced Small Form-factor Pluggable (SFP+) fiber-optic transceiver module that uses a wavelength of 850 nm and operates at speeds of at least 6.6 Gbps.
Justification: This is the form factor that is used by the upgraded STP2 network, which is used for the fast readout of triggered events.
Status: Tested and working.
11) Requirement: **Extra SFP+ Cages.** The DSM2 must include 4 more SFP+ cages that can accept pluggable SFP+ fiber-optic transceiver modules.
Justification: These transceivers will be used to transmit data between DSM2 boards.
Status: Tested (in packet-mode, not streaming) and working. NOTE: The system needed to stream data constantly over high-speed serial links is different from the system used to send occasional packets at random times (e.g. for readout after a trigger has been issued). Tests of a set of hardware and firmware for constant streaming were started using the TRP module, but not completed. The results obtained so far indicate that a solution using the STP2 hardware but different firmware is most likely possible. For the DSM2 it was therefore decided to include the same 4-unit cage and its

associated receptacles that are used on the STP2R and STP2C boards. These parts are low cost so including them in the board design maintains the possibility of implementing high-speed serialized streaming I/O with very little risk. If the firmware development is successful then the transceiver parts can be purchased and installed.

12) Requirement: **Data Storage**. The DSM2 must have at least as much on-board memory as the existing DSM boards. Those boards use 16-bit addresses for their memory and store 160 bits (128 inputs + 32 outputs) at each address making 2^{16} x 160 = 10.5 Mb in total. The memory access scheme must allow at least two accesses during each RHIC clock tick.
    Justification: The decision to issue a trigger and read out the data is made downstream of the DSM tree by the TCU. There is therefore a delay between when data is received by any DSM2 and when it is read out. The DSM2 must store the data while it waits for the trigger decision to be made. When the TCU does issue a trigger it currently includes a 16-bit address pointer in the trigger information which the DSM2 must use to read the correct data from its memory. During normal data taking new data will be stored in the memory every tick of the RHIC clock. At random times, when a readout command has been received, it will also be necessary to read out data from the memory. The memory access scheme must therefore allow at least two accesses during each RHIC clock tick.
    Status: Tested and working. DSM2 uses the same 4 Gb DDR3 SDRAM that is used on the STP2R boards, which is more than enough to duplicate what is on the existing DSM boards and also leaves room for future expansion.
13) Requirement: **Field-Programmable Logic**. All of the firmware for implementing the trigger algorithms, accessing the memory, processing fast readout requests, etc… must be implemented in a field-programmable gate array (FPGA). The firmware must be stored in non-volatile, re-programmable memory on the DSM2.
    Justification: The details of the DSM2 logic will need to be modified over time (e.g. for use with different algorithms) so it must be re-programmable. However, the DSM2 boards will sometimes be power-cycled for reasons that have nothing to do with logic changes. In that case the existing logic should just be reloaded from non-volatile memory.
    Status: Tested and working. DSM2 uses the same FPGA with the same flash memory that are used on the STP2R.
14) Requirement: **Remote Reset**. The DSM2 must have a remotely-accessible reset path to reset all logic to the power-on state.
    Justification: Sometimes an error occurs that results in a board freezing up. Since STAR is not physically accessible during data taking initiating the reset must be done remotely.
    Status: Tested and working. The FPGA on DSM2 can be reset using the VME SYSRESET line or a dedicated line from the ConnectCore ™ module.
15) Requirement: **Front Panel Clock Monitor**. The DSM2 boards must each drive the RHIC clock to an output connector located on the front panel.
    Justification: This is necessary to check that the clock has the expected frequency and duty-cycle and that it is properly synchronized across multiple boards
    Status: Tested and working. The FPGA can drive the selected clock to a Lemo connector on the front panel.

16) Requirement: **Front Panel Indicators**. The DSM2 boards need front panel LEDS to monitor the primary voltage (3.3V), FPGA configuration state, clock source (RCC2 or local oscillator) and the primary RCC2 control signal (run/stop). There should be at least one additional (spare) LED that can be controlled from the FPGA.
Justification: During testing and debugging this is the easiest way to monitor these features.
Status: Tested and working.
17) Requirements: **Test Points**. The DSM2 boards need test points connected to GND (for scope probes), each power supply (to check voltages) and a few FPGA pins.
Justification: This makes testing and debugging much simpler.
Status. Tested and working.

Firmware

18) Requirement: **Ethernet Communications**. The DSM2 firmware must include a path for Ethernet-based communication.
Justification: This is how the user will control and monitor the board.
Status: Tested and working. This firmware module is closely based on the version used by STP2R.
19) Requirement: **Configuration Memory Interface**. The DSM2 firmware must include an interface to the non-volatile, re-programmable memory that holds the FPGA configuration data.
Justification: The combination of an Ethernet interface and a flash memory interface will enable the user to download new FPGA configuration files remotely, i.e. without having to use the JTAG interface.
Status: Tested and working. This firmware module is the same as the version used by STP2R.
20) Requirement: **STP2 Transceiver Interface**. The DSM2 firmware must be capable of receiving/transmitting packets of data from/to the STP2 optical transceiver.
Justification: Requests for the readout of triggered data will be received from the STP2 Concentrator through this transceiver and the data must be sent back to the STP2 Concentrator through the same transceiver.
Status: Under development.
21) Requirement: **Data Storage Interface**. The DSM2 firmware must include an interface to the data storage memory that allows for at least these 4 modes of operation:
    a. When the board is in RUN mode during normal data taking all 128 input bits and 32 output bits must be written to the memory every tick of the RHIC clock.
    b. When the board is in RUN mode and a test is in progress simulated data must be read from the memory every tick of the RHIC clock.
    c. When a fast readout request has been received the requested data must be read from the memory without interfering with the regular writes/reads of modes a) and b).
    d. Read/write access to any memory location must be possible under Ethernet control, also without interfering with either the regular writes/reads of modes a) and b) or the occasional reads of mode c)

Justification: Modes a) and c) are needed for normal data taking operations. Mode b) is useful for board and system testing and mode d) is useful for setting up test data and checking the results.
Status: Under development.

22) Requirement: **Data Flow Control**. The DSM2 firmware must allow the user to select which data source is used for the algorithm input (data from P3, data from the Extra SFP+ transceivers or test data) and which data set is driven to the output on P2 (algorithm result or test data).
Justification: These different modes of operation are required for normal data taking and for various test purposes.
Status: Under development.

23) Requirement: **Data Storage Control**. During data taking the DSM2 firmware must use the STAR synchronous RUN/STOP signal to control when and at which address access to the memory should begin. It must also respond to the STAR synchronous "latch address" command and have the potential to respond to what is currently the spare command.
Justification: Every board in the Trigger System has an address counter that increments by one every tick of the RHIC clock. This counter determines where to store the current data in the memory. The RUN/STOP command is distributed simultaneously throughout Trigger System by the RCC2. All the boards use this signal in the same way to start incrementing their address counters and this ensures that the address counters remain synchronized to each other. Data from a specific RHIC bunch crossing will be stored in the same memory location across all the boards. This information is used to determine which data to read out once a trigger has been issued. The "latch address" command is used for monitoring purposes, to check that all the boards are still synchronized. The spare may be used in the future.
Status: Under development.

24) Requirement: **Data Readout Control**. When a packet is received from the local STP2 transceiver (requirement #10) the DSM2 firmware must first check that it contains a valid BUILD_EVT command. If so it must extract the data address from the packet, read the data at that address from the memory and then create a new packet of data that is transmitted by that STP2 transceiver. The firmware must allow the user to specify which of the available data bits (input, output, etc…) are to be transmitted in the outgoing packet. This could involve either decoding another field from the BUILD_EVT packet or using information specified by the user during configuration. When the outgoing packet is created the bits must be stored in the same order that is produced by the existing DSM boards.
Justification: The data must be read out in order to understand why each trigger was issued. Providing the option of reading out the output data has been found to be necessary for debugging purposes. In theory the output of any DSM board is known because it is always used as the input to the next board in the tree. However, in practice in the existing system there have been several occasions where the data received by the downstream board is incorrect. This could be due to either a firmware problem, or a hardware problem in the board-to-board link. Reading the output data from any DSM board would allow the user to distinguish between these two options, but that is not possible in the existing system. Maintaining the existing bit order is required because

there is a huge amount of downstream software (both online and offline) that is dependent on the existing bit order and would be very hard to change.
Status: Under development.

25) Requirement: **Input Data Latch**. The DSM2 firmware must latch the incoming data from P3 or the Extra SFP+ transceivers (after the serial SFP+ data has been parallelized) once per tick of RHIC clock.
Justification: The incoming data bits will arrive at slightly different times due to differences in upstream detector hardware, cable lengths and routing. Those bits must be held in a stable state while the algorithm logic operates.
Status: Under development. **NOTE**: On the existing DSM boards this latch was implemented in discreet ICs on the PC board, which will now not be necessary.

26) Requirement: **Channel Mask**. The DSM2 firmware must include registers to allow the user to turn on or off each channel (group of input bits) in the downstream logic.
Justification: Occasionally a part of the upstream hardware breaks resulting in noisy or stuck bits being received by the DSM system. Since STAR is not physically accessible during data taking it is often not possible to fix the hardware in a timely fashion, so those problems have too be fixed in firmware.
Status: Under development. **NOTE**: On the existing DSM boards this mask was implemented as look-up tables in memory chips on the PC board, which will now not be necessary.

27) Requirement: **Data Analysis**. The DSM2 firmware must analyze all the incoming data using user-provided algorithms.
Justification: These algorithms check to see if an interesting interaction occurred, and that information will be used to make the trigger decision.
Status: Under development. **NOTE**: All of the algorithm VHDL code from the existing DSM boards exists in a form that is largely independent of the control and infrastructure VHDL code. As a result adapting the existing algorithm code to the new DSM2 boards will be an easy task involving just minor modifications.

28) Requirement: **Output Data Delay**. The DSM2 firmware must delay its output by a user-specified number of clock ticks. The maximum delay is 10 RHIC clock ticks.
Justification: Data from different detectors arrives at the DSM System at very different times, i.e. in different ticks of the RHIC clock. Data from early detectors must be delayed to wait for data from later detectors before the data reaches the TCU. The DSM2 therefore needs to have the delay capability.
Status: Under development. **NOTE**: On the existing DSM boards this delay was implemented in discreet FIFO ICs on the PC board, which will now not be necessary.

29) Requirement: **Readout Monitor**. During data taking the DSM2 firmware must use the synchronous RUN/STOP signal to start a counter that counts RHIC clock ticks and is large enough that its value will never wrap around to zero during a STAR run. Its value must be saved immediately after data has been read from the memory during readout.
Justification: The TCU has an equivalent counter whose value is saved whenever a trigger is issued. These counters will allow the user to monitor the time between when a trigger was issued and when the data was read out.
Status: Under development. **NOTE**: In the current system this functionality is implemented on the RCC2 and the counter value is read by the VME CPU after it has

read out all of the DSM boards in that crate. In the new system that will not be necessary.

30) Requirement: **Input Timing Monitor**. The DSM2 firmware must use a high-frequency clock that is independent of the RHIC clock to measure the time between when a selected input bit changes value and when the Input Data Latch occurs.
Justification: Each layer of the DSM tree operates on a different phase of the RHIC clock. Sometimes it is necessary to adjust the clock phase for a board to make sure that it can properly receive data from the upstream layers and send data to the downstream layers without having any setup or hold timing violations. Monitoring the time between data and latch transitions will make those adjustments easier.
Status: Under development.

31) Requirement: **Configuration Time**. The total time to configure the DSM2 must be substantially less than the time taken to configure the Time Projection Chamber (TPC) subsystem. For the DSM2 this includes the time to set all FPGA registers. It does not include the time to download a new FPGA configuration.
Justification: STAR needs to minimize the time taken to configure the full system in order to maximize the amount of data-taking time. The Trigger subsystem is always configured before the TPC in order to ensure that the clocks that the Trigger provides to the TPC are in their correct state when the TPC configuration starts. If the time to configure the Trigger is substantially less than the time to configure the TPC then the Trigger avoids being the configuration bottleneck. All of the DSM2 boards will be configured in parallel, each one using its own Ethernet connection, so the time to configure the Trigger will depend on the time to configure one DSM2. During normal data-taking configuring a DSM board involves (re)setting user registers and counters, all of which can be done quickly and efficiently, Downloading a new FPGA configuration is more time consuming, but STAR has matured to the point where that is typically only done when beam-species or collision energy changes so it will not be part of the typical configuration process.
Status: Under development.