The Cabling Scheme and DSM Algorithms for the EMC Trigger For the 2018 200 GeV Heavy Ion Run

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Change Log:

Date	Description
March 6, 2014	First complete version for 2014. The logic for the 2014 heavy-ion run is very different from the logic used over the previous few years. The jet patch logic has been removed entirely to make room for more high-tower and trigger patch-based topology triggers.
March 11, 2014	Second complete version for 2014, implemented with the "b" versions of all the BEMC algorithms and the EM201 algorithm. I added a 6^{th} HT threshold and propagated it through the system. In order to make room for the extra output bit at layer-2 the various UPC topology bits were combined, with a register to switch individual elements on and off.
February 27, 2018	First version for 2018. The BEMC is still using the 2014_b heavy ion algorithms. The EEMC is using algorithms developed in 2017 for the proton-proton running, which includes extra registers for the HT.TP logic. There is a new EM201 algorithm for 2018, which adds the EEMC into the existing HT.TP topology logic. The HT.TP logic has also been simplified: the non-adjacent logic has been removed, leaving only the back-to-back topology bit

Eta-Phi Coverage

The EMC trigger is set up operate on fixed jet patches that overlap in eta but not in phi. The detector is connected to the DSM tree in such a way that each BEMC layer 0 DSM board receives ADC information from each of 10 trigger patches. Each trigger patch covers a region of eta-phi space measuring (0.2x0.2). The assignment of trigger patches to layer 0 DSM boards is done so that each layer 0 DSM board covers a region measuring (1x0.4).

This is illustrated in Figure 1, which shows a (2x2) region of eta-phi space. The thin solid lines indicate which areas are connected to each layer 0 DSM board. There are 10 layer 0 DSM boards in this diagram; 5 at negative eta and 5 at positive eta. The thick lines indicate which areas are then connected to each layer 1 DSM board. The dashed lines (both thick and thin) show how each layer 0 DSM board can split its trigger patches into sub-groups.

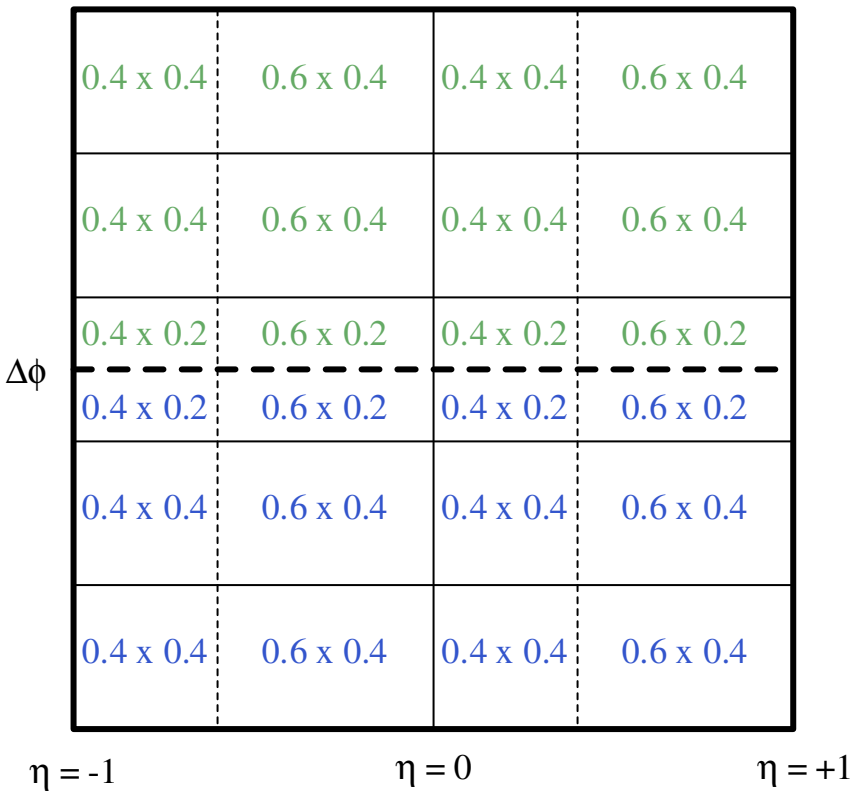

Figure 1: The BEMC DSM Eta-Phi Scheme

It can be seen that the two DSM boards covering the central phi region can actually split their patches into four small groups, covering either a (0.6x0.2) region or one measuring (0.4x0.2). The other eight DSM boards split their patches into just two groups, making a (0.6x0.4) region and a (0.4x0.4) region. Each DSM board can put a 6-bit sum from each of two groups onto one output cable. This means the two DSM boards covering the

central phi region can use both output cables to pass on the sums from all four of their groups.

BEMC Cabling Detail

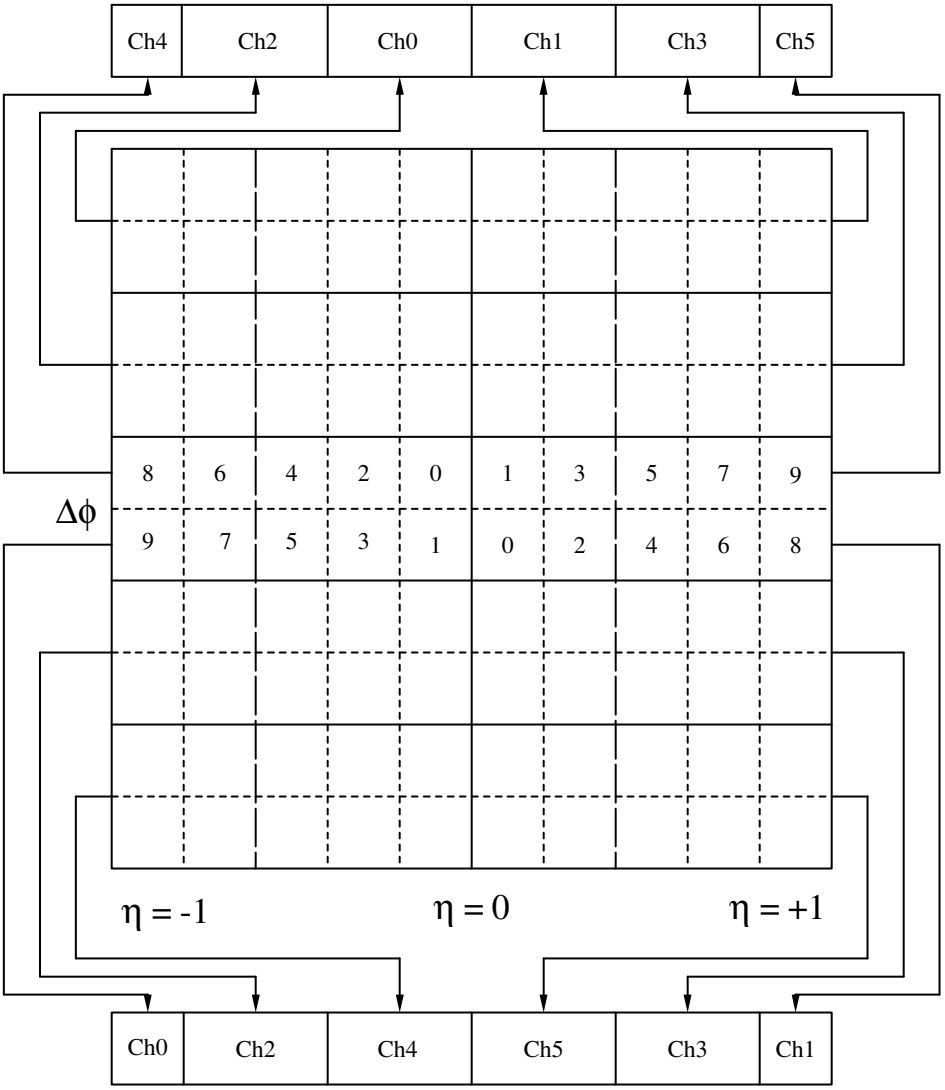

Figure 2: BEMC Cabling Scheme

The layer-0 to layer-1 connections are then arranged so that at a given phi value the positive and negative eta regions all go to the same layer 1 DSM board. Figure 2 shows the detail of the cabling scheme. As in Figure 1, the diagram shows the (2x2) region of eta-phi space. The solid lines indicate which areas are connected to each layer 0 DSM board and the dashed lines outline the individual trigger patches. The long-dashed lines show how each layer 0 DSM can split its channels into two eta groups. In the central phi region, the numbers show how the trigger patches are connected to the ten input channels of the layer 0 DSM boards.

The sidebars show how the layer 1 DSM boards are connected to the layer 0 boards so that each one receives data from both East and West sides of the detector. It can be seen that the two output cables from the DSM boards covering the central phi region go to different layer 1 DSM boards. The East-side layer-0 DSM boards connect to the even-numbered channels of the layer-1 boards, and the West-side layer-0 boards connect to the odd-numbered channels. It can be seen that there is a difference in the cabling of the upper (in this diagram) and lower layer-1 DSM boards. The upper layer-1 DSM board receives data from the single–output layer 0 DSM boards on channels 0:3, and the data from the double-output boards on channels 4 and 5. The lower layer-1 DSM board receives the data from the double-output boards on channels 0 and 1, and the single-output boards on the other channels. Since the format of the data is always the same the cabling difference does not matter, and all of the layer-1 DSMS are able to use the same algorithm.

Every layer-1 DSM board therefore receives input from an eta-phi area measuring (2x1) in total. Each layer-1 DSM board therefore covers a full 2-hour pie-slice of the BEMC barrel. It can combine the sums to make three overlapping (1x1) jet patches. It can also make a partial jet patch that can be completed at layer-2 using data from the EEMC DSM tree. This eliminates acceptance gaps in eta, but leaves acceptance gaps in phi.

For the 2014 heavy ion run there are no plans to trigger on the jet patches, so the sums do not need to be calculated. The plan instead is to trigger on back-to-back (or non-adjacent) combinations of hits as part of an effort to look for J/Ψ particles from ultra-peripheral collisions. The definition of a “hit” could be either a high tower over a threshold or an entire trigger patch over a threshold or both. The logic tree makes an OR of the necessary information within the layer-0 and layer-1 DSM boards, and the results are all passed to the layer-2 DSM board. That final board then combines the bits to search for the interesting topologies.

BEMC Layer-0 Algorithm Description

At layer-0 the logic must OR the high tower (HT) and trigger patch (TP) threshold bits. The difference in the cabling of trigger patches into the single-output layer-0 DSM boards between the East and West side does not affect the result of an OR. The single-output DSM boards can therefore all use the same algorithm. However, the difference in cabling does matter for the double-output DSM boards. Those DSM boards switch their output mapping between the East and West sides. Two algorithms will therefore be needed for the double-output DSM boards; one for the East side and one for the West side.

Single-output DSM

- RBT File: bemc_be001_2014_b.rbt
- Users: BE001:BE002, BE004:BE007, BE009:BE012, BE014:BE105, BW001:BW002, BW004:BW007, BW009:BW012, BW014:BW105
- Input: 10 BEMC channels:
    - bits 0:5 = high tower (HT)
    - bits 6:11 = trigger patch (TP)
- LUT: 1-to-1 mapping. Missing, dead and noisy channels are also zeroed out here.
- Registers: Seven registers, each containing one 6-bit threshold value. NOTE: these are NOT size ordered.
    - R0: BEMC-HT-th0 (6 bits)
    - R1: BEMC-HT-th1 (6)
    - R2: BEMC-HT-th2 (6)
    - R3: BEMC-HT-th3 (6)
    - R4: BEMC-HT-th4 (6)
    - R5: BEMC-HT-UPC (6)
    - R6: BEMC-TP-UPC (6)
- Step 1: Latch input.
- Step 2: Compare each HT value to all 6 thresholds.
  Compare each TP value to the single TP threshold.
- Step 3: For each HT threshold, combine (OR) the HT bits from all 10 channels
  Combine (OR) the TP bits from all 10 channels.
  Combine (AND) the TP and HT-UPC bits for each channel and then OR the results for all channels together, i.e.

  HT.TP = (TP(0) and HT-UPC(0)) or
  (TP(1) and HT-UPC(1)) or
  …
  (TP(9) and HT-UPC(9))
- Step 4: Latch output
- Output to Layer-1 DSM
    - bits 0-7 Unused
    - bit 8 TP threshold bit
    - bit 9 HT.TP threshold bit
    - bits 10-15 HT threshold bits (NOTE: HT-UPC is the MSB)

Double-output East

- RBT File: bemc_be003_2014_b.rbt
- Users: BE003, BE008, BE013
- Input: Same as Single-output DSM algorithm
- LUT: Same as Single-output DSM algorithm
- Registers: Same as Single-output DSM algorithm
- Step 1: Latch input.
- Step 2: Same as Single-output DSM algorithm
- Step 3: Combine (OR) the HT bits from the even-numbered input channels and the odd-numbered input channels separately.
  Combine (OR) the TP bits from the even- and odd-numbered channels separately.
  Combine (AND) the TP and HT-UPC bits for each channel and then OR the results for the even- and odd numbered channels separately.
- Step 4: Latch output.
- Output to Layer-1 DSM
  - bits 0-7 Unused
  - bit 8 TP threshold bit from even-numbered channels
  - bit 9 HT.TP threshold bit from even-numbered channels
  - bits 10-15 HT threshold bits from even-numbered channels
  - bits 16-23 Unused
  - bit 24 TP threshold bit from odd-numbered channels
  - bit 25 HT.TP threshold bit from odd-numbered channels
  - bits 26-31 HT threshold bits from odd-numbered channels

Double-output West

- RBT File: bemc_bw003_2014_b.rbt
- Users: BW003, BW008, BW013
- Input: Same as Single-output DSM algorithm
- LUT: Same as Single-output DSM algorithm
- Registers: Same as Single-output DSM algorithm
- Step 1: Latch input.
- Step 2: Same as Single-output DSM algorithm
- Step 3: Same as double-output East algorithm
- Step 4: Latch output with the REVERSE even-odd ordering from the East algorithm.
- Output to Layer-1 DSM
  - bits 0-7 Unused
  - bit 8 TP threshold bit from odd-numbered channels
  - bit 9 HT.TP threshold bit from odd-numbered channels
  - bits 10-15 HT threshold bits from odd-numbered channels
  - bits 16-23 Unused
  - bit 24 TP threshold bit from even-numbered channels
  - bit 25 HT.TP threshold bit from even-numbered channels
  - bits 26-31 HT threshold bits from even-numbered channels

BEMC Layer 1 Algorithm Description

There is just one layer-1 algorithm for the BEMC, which will be used by all 6 DSM boards.

- RBT File: bemc_bc101_2014_b.rbt
- Users: BC101:BC106
- Input: 6 channels, each with the format
  - bits 0-7 Unused
  - bit 8 TP threshold bit
  - bit 9 HT.TP threshold bit
  - bits 10-15 HT threshold bits (NOTE: HT-UPC is the MSB)
- LUT: 1-to-1 mapping
- Registers: One register. The register selects one of the six HT bits from each channel to be passed to EM202
  - R0: BEMC_DAQ10k_HT_Sel (3)
    0 => select HT-th0 information for DAQ10k
    1 => select HT-th1 information for DAQ10k
    Etc…
    5 => select HT-UPC information for DAQ10k

Step 1: Latch input.

- Step 2: Combine (OR) the HT bits from input channels 0:2 and 3:5 separately.
  Do the same for the TP and HT.TP bits.
  Use the register to select one of the six HT bits from each of the 6 input channels for the DAQ10k readout.
  Combine (OR) those 6 bits to make the DAQ10k test bit.
- Step 3: Combine (OR) the two intermediate groups of HT bits together.
  Do the same for the TP and HT.TP bits.
  Delay the 6 HT bits selected for the DAQ10k logic, and the DAQ10k test bit to the 4^{th} step.
- Step 4: Latch output.
- Output to EM201:
  - bits 0-6 Unused
  - bit 7 DAQ10k test bit
  - bit 8 TP threshold bit
  - bit 9 HT.TP threshold bit
  - bits 10-15 HT threshold bits (NOTE: HT-UPC is the MSB)
- Output to EM202:
  - bits 16-21 DAQ10k HT bits
  - bits 21-31 Unused

EEMC Cabling Detail

Figure 3 shows how the EEMC trigger patches are connected to the layer 0 DSM boards, as seen from the West looking towards the center of STAR. The thick solid lines indicate which areas are connected to each layer 0 DSM board. The thin dashed lines outline the individual trigger patches. A pair of adjacent jet patches is highlighted. The numbers indicate which layer 0 DSM board channel is connected to each trigger patch.

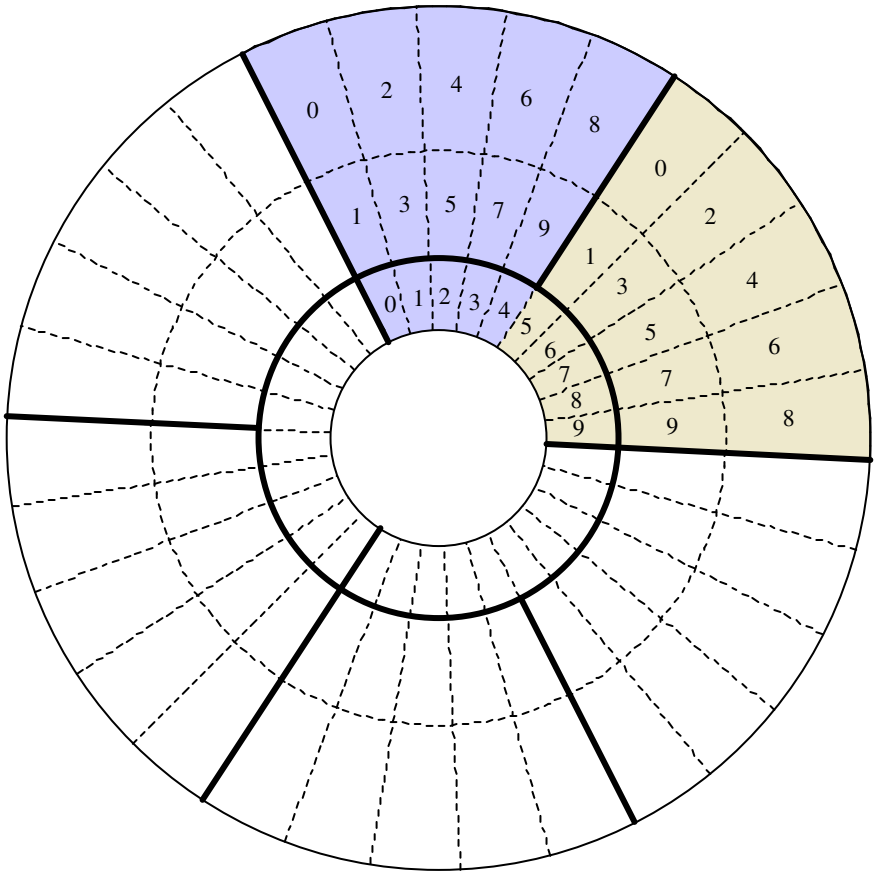

Figure 3: EEMC DSM Eta-Phi Scheme, seen from the West looking towards the center of STAR

It can be seen that every EEMC (1x1) jet patch is split between two layer 0 DSM boards. In each case, the 10 outer trigger patches (lowest eta) are connected one layer 0 DSM board, and the 5 inner trigger patches (highest eta) are connected to another layer 0 DSM board. That second board also contains the five inner trigger patches for the adjacent jet patch. In this cabling scheme the boards that cover the outer trigger patches each have one output cable. The boards that cover the inner trigger patches of two jet patches have two output cables. The result is twelve cables which are split between two layer 1 DSM boards in such a way that each of the layer 1 DSM boards covers half of the EEMC.

The aim of the cabling scheme is to make (1x1) jet patches that overlap in eta. The EEMC only covers one unit of eta so all that is possible is to make one internal (1x1) jet patch and a partial (0.4x1) jet patch on the EEMC-BEMC boundary that can be combined with the partial jet patch (JPpartial) from the BEMC side of the boundary. The EEMC cabling scheme is therefore set up to construct (1x1) jet patches with the same phi range as in the BEMC. The partial (0.4x1) jet patch is constructed by summing together the even numbered channels of the single-output layer 0 DSMS (which cover the low eta part of the EEMC).

The EEMC layer-0 algorithms differ from the jet-patch BEMC algorithms primarily in the definition of which groups of channels are added together to make the TP sums. The single-output EEMC layer 0 DSM boards add together the even-numbered (low eta) channels in one group, and the odd-numbered (high-eta) channels in another group. The low eta group forms the partial jet patch that can be combined with the BEMC partial jet patch at layer-2. The double-output EEMC layer 0 DSM boards add together channels 0:4 in one group, and channels 5:9 in the other (as indicated in Figure 3). However, there is an additional difference associated with the pedestal subtraction. The BEMC layer-0 algorithms do the pedestal subtraction such that each TP sum is left with a residual pedestal of 1. Six TP sums are added together to make a jet patch, so the BEMC jet patch pedestal value is 6. Only three TP sums are added together to make the partial jet patch (JPpartial), so it's pedestal value is 3. In order to simplify later analysis it would be useful to ensure that all jet patches, including those that come from the EEMC and the BEMC-EEMC boundary, also have a pedestal value of 6. To this end, the pedestal subtraction in the EEMC layer 0 algorithms is done as shown in Table 1. Note that "N" is still the number of channels that are added together to make the TP sum, just like in the BEMC logic. In the case of the EEMC algorithms, "N" is always 5.

Table 1: TP sum Pedestal Calculations in the EEMC Layer 0 Algorithms

TP Sum	Pedestal Subtraction Equation	Residual Pedestal
Low eta sum from single-output DSM	TPsum = TPsum-(N-3)	3
High eta sum from single-output DSM	TPsum = TPsum-(N-2)	2
Sum from double-output DSM	TPsum = TPsum-(N-1)	1

When the three sums listed in Table 1 are added together to make an internal EEMC jet patch the total pedestal value of the jet patch is 6, which matches the BEMC. When the low eta sum from the single-output DSM is added to JPpartial, from the BEMC, to complete the boundary-spanning jet patch, the total pedestal for that jet patch also comes to 6, again matching the BEMC.

The EEMC layer-0 and layer-1 algorithms for 2014 are unchanged from the previous years, i.e. they still calculate the jet patch sums. This is because those algorithms also already provide all the HT bits needed for triggering. The jet patch information will be ignored at layer-2.

EEMC Layer 0 Algorithm Description

Single-output (Low Eta)

- RBT File: eemc_ee001_2017_b.rbt
- Users: EE001, EE003, EE004, EE006, EE007, EE009
- Input: 10 EEMC channels: bits 0:5 = high tower, bits 6:11 = trigger patch
- LUT: Pedestal subtraction and energy calibration is done in the EEMC read-out electronics. Therefore the LUT's are mostly 1-to-1. Missing, dead and non-instrumented channels are zeroed out here.
- Registers: Four 6-bit registers, three for the high tower comparison and one for the trigger patch comparison. These are NOT size ordered.
    - R0: EMC_EEMC_HT_th0 (6 bits)
    - R1: EMC_EEMC_HT_th1 (6)
    - R2: EMC_EEMC_HT_UPC (6)
    - R3: EMC_EEMC_TP_UPC (6)
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Steps 2 and 3 combined: NOTE that this merged step is given 2 ticks of the clock to complete.
    - Sum the five even numbered (low eta) TP channels and the five odd numbered (high eta) channels separately. Subtract the pedestal from each TP sum. The pedestal subtraction equations are described in Table 1. If the initial TP sum is less than N (5), then the result of the pedestal subtraction process shall be zero. Next, select the lower 6 bits of each pedestal-subtracted TP sum. Set all 6 bits high (63) if any higher-order bits are set in the pedestal-subtracted sum.
    - In parallel with the sum logic, compare each HT value to its 3 thresholds and each TP value to its single threshold. Combine (OR) the th0 and th1 HT bits from all channels. Make the HT.TP bit for each channel by combining (AND) the HT-UPC and TP-UPC bits, and then OR the results from all 10 channels.
- Step 4: Send the two 6-bit TP sums (low and high eta), the 2 HT bits and the 1 HT.TP bit to layer 1 on one output cable.

Double-output (High Eta)

- RBT File: eemc_ee002_2017_b.rbt
- Users: EE002, EE005, EE008
- Input: Same as Single-output (Low Eta)
- LUT: Same as Single-output (Low Eta)
- Registers: Same as Single-output (Low Eta)
- Step 1: Receive the 6-bit high tower (HT) and trigger patch (TP) information from each of ten trigger patches.
- Steps 2 and 3 combined: NOTE that this merged step is given 2 ticks of the clock to complete.

    - Sum the TP channels in two groups: (0:4) and (5:9). Subtract the pedestal from each TP sum using the equation from Table 1, and then select the lower 6 bits, as in the single-output (low eta) algorithm.
    - In parallel with the sum logic, compare each HT value to its 3 thresholds and each TP value to its single threshold. Combine (OR) the th0 and th1 HT bits from channels (0:4) and (5:9) separately. Make the HT.TP bit for each channel by combining (AND) the HT-UPC and TP-UPC bits, and then OR the results from channels 0:4 and 5:9 separately.
- Step 4: Send the 6-bit sum, the 2 HT bits and the 1 HT.TP bit from channels (0:4) to layer 1 on the first output cable. On the cable, the sum will be in the bit range used by the low-eta sum in the single-output algorithm. The bits assigned to the high-eta sum will be set to zero. Send the data from channels (5:9) to layer 1 on the second output cable.

In both algorithms the output data on each cable have similar formats, as shown in Table 2:

Table 2: Output of Layer 0 EEMC DSM Boards

Data	Bit Range	Bit Count	Bit Total
TP sum for low-eta group	0:5	6	16
TP sum for high-eta group (N/A, set to zero, for the double-output algorithm)	6:11	6	
HT bits	12:13	2	
Unused	14	1	
HT.TP bit	15	1	

EEMC Layer 1 Algorithm Descriptions

The two EEMC layer 1 DSM boards have slightly different algorithms due to a feature of the layer-0 to layer-1 connection scheme. These connections are shown in Figure 4. As in Figure 3, the thick solid lines indicate which areas are connected to each layer 0 DSM board. The dashed lines show how the inner regions are split by the layer 0 DSM boards to make pieces of two adjacent jet patches. The arrows show how the outputs of the layer 0 DSM boards (including both outputs from the double-output boards) connect to the input channels of the two layer 1 DSM boards.

It can be seen that the layer 1 DSM board covering the bottom half of the EEMC (EE101) receives data from the outer (low eta) parts of its jet patches on input channels 0, 3 and 4. It is therefore these channels that will provide the partial jet patch information that needs to be passed up to layer 2. However, the layer 1 DSM board covering the upper half of the EEMC (EE102) receives data from the outer parts of its jet patches on input channels 1, 2 and 5, so it is these channels that will provide the partial jet patch information. The two layer 1 DSM board algorithms are therefore slightly different, to account for this difference in the input mapping.

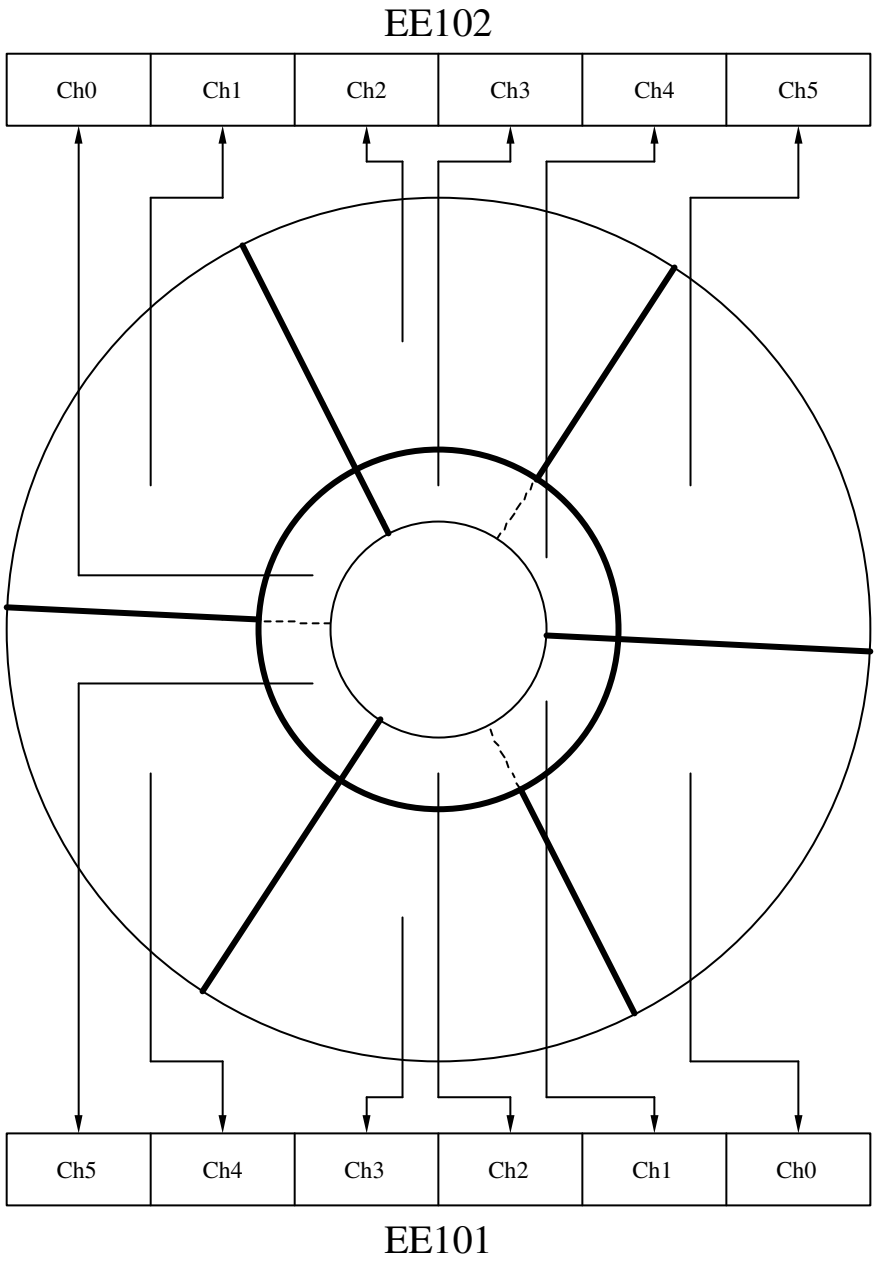

Figure 4: The EEMC Cabling Scheme, with the Endcap seen from the West looking toward the center of STAR.

Lower Half (EE101)

- RBT File: eemc_ee101_2017_a.rbt
- User: EE101
- Input: 6 channels, each with the format given in Table 2 (see Page 11)
- LUT: 1-to-1 mapping

- Registers: Three registers, each containing one 8-bit threshold value for the jet patch comparison. As in the past, these are SIZE-ORDERED, so th0 < th1 < th2
    - R0: EMC_EEMC_JP_th0 (8 bits)
    - R1: EMC_EEMC_JP_th1 (8)
    - R2: EMC_EEMC_JP_th2 (8)
- Step 1: Receive two 6-bit TP sums (low and high eta), 2 HT bits and 1 HT.TP bit on each of six cables. Three of these cables (channels 0, 3 and 4) come from single-output layer 0 DSM boards. The other three cables (channels 1, 2 and 5) come from double-output layer 0 DSM boards, and on those cables the second 6-bit TP sum will always be zero. The sums will be referred to as ChX_{LO} and ChX_{HI} to indicate which channel, and which eta range, are being selected.
- Step 2: Calculate 3 jet patches sums as follows:
    - JPA (4 o'clock) = $Ch0_{LO} + Ch0_{HI} + Ch1_{LO}$
    - JPB (6 o'clock) = $Ch3_{LO} + Ch3_{HI} + Ch2_{LO}$
    - JPC (8 o'clock) = $Ch4_{LO} + Ch4_{HI} + Ch5_{LO}$

  Also calculate an HT.TP bit from each jet patch:
    - HTTP-A (4 o'clock) = HT.TP-Ch0 or HT.TP-Ch1
    - HTTP-B (6 o'clock) = HT.TP-Ch2 or HT.TP-Ch3
    - HTTP-C (8 o'clock) = HT.TP-Ch4 or HT.TP-Ch5

  In parallel, compare pairs of the low eta sums arriving from the single-output layer 0 DSM boards (i.e. $Ch0_{LO}$, $Ch3_{LO}$ and $Ch4_{LO}$). Also combine (OR) the HT bits from input channels 0:2 and 3:5 separately.
- Step 3: Combine (OR) the two intermediate groups of HT bits together. Delay the HT.TP bits to Step 4. Compare each of JPA, JPB and JPC to the three thresholds, combine (OR) the results from all 3 jet patches and then pack the results into a single 2-bit integer. Combine the results of the 2-channel comparisons (calculated at Step 2) to select the largest low eta sum.
    - A (4 o'clock) = ($Ch0_{LO} > Ch3_{LO}$) and not ($Ch4_{LO} > Ch0_{LO}$)
    - B (6 o'clock) = ($Ch3_{LO} > Ch4_{LO}$) and not ($Ch0_{LO} > Ch3_{LO}$)
    - C (8 o'clock) = ($Ch4_{LO} > Ch0_{LO}$) and not ($Ch3_{LO} > Ch4_{LO}$)

  This is the partial jet patch that will be sent on to layer 2. Note that if all three low eta sums are the same (e.g. in an event where nothing happens) then all three comparisons will be false. In this case, sum A, at 4 o'clock, is selected. Use a 2-bit integer to indicate which of the three sums has been selected.
    - 1 = A (4 o'clock)
    - 2 = B (6 o'clock)
    - 3 = C (8 o'clock)

Step 4: Send to layer 2: the HT.TP bit from each of the 3 jet patches, the 2-bit integer for the combined completed jet patches, the 6 bits of selected partial jet patch sum, its 2-bit ID and the 2 HT bits. The output data format is shown in Table 3.

Table 3: Output of Layer 1 EEMC DSM Boards

Data	Bit Range	Bit Count	Total
JP threshold bits	0:1	2	16
HT.TP-A bit	2	1	

HT.TP-B bit	3	1	
HT.TP-C bit	4	1	
Unused	5	1	
Selected partial jet patch sum	6:11	6	
Partial jet patch ID	12:13	2	
HT bits	14:15	2	

Upper Half (EE102)

- RBT File: eemc_ee102_2017_a.rbt
- User: EE102
- Input: Same as Lower Half (EE101)
- LUT: Same as Lower Half (EE101)
- Registers: Same as Lower Half (EE101)
- Step 1: Receive two 6-bit TP sums (low and high eta), 2 HT bits and 1 HT.TP bit on each of six cables. Three of these cables (channels 1, 2 and 5) come from single-output layer 0 DSM boards. The other three cables (channels 0, 3 and 4) come from double-output layer 0 DSM boards, and on those cables the second 6-bit TP sum will always be zero. Note that this mapping is exactly the opposite of the mapping into the first layer 1 DSM board (EE101).
- Step 2: Calculate 3 jet patches sums as follows:
    - JPA (10 o'clock) = $Ch1_{LO} + Ch1_{HI} + Ch0_{LO}$
    - JPB (12 o'clock) = $Ch2_{LO} + Ch2_{HI} + Ch3_{LO}$
    - JPC (2 o'clock) = $Ch5_{LO} + Ch5_{HI} + Ch4_{LO}$

  Also calculate an HT.TP bit from each jet patch:
    - HTTP-A (10 o'clock) = HT.TP-Ch0 or HT.TP-Ch1
    - HTTP-B (12 o'clock) = HT.TP-Ch2 or HT.TP-Ch3
    - HTTP-C (2 o'clock) = HT.TP-Ch4 or HT.TP-Ch5

  In parallel, compare pairs of the low eta sums arriving from the single-output layer 0 DSM boards (i.e. $Ch1_{LO}$, $Ch2_{LO}$ and $Ch5_{LO}$). Also combine (OR) the HT bits from input channels 0:2 and 3:5 separately.
- Step 3: Combine (OR) the two intermediate groups of HT bits together. Delay the HT.TP bits to Step 4. Compare each of JPA, JPB and JPC to the three thresholds, combine (OR) the results from all 3 jet patches and then pack the results into a single 2-bit integer. Combine the results of the 2-channel comparisons (calculated at Step 2) to select the largest low eta sum.
    - A (10 o'clock) = ($Ch1_{LO} > Ch2_{LO}$) and not ($Ch5_{LO} > Ch1_{LO}$)
    - B (12 o'clock) = ($Ch2_{LO} > Ch5_{LO}$) and not ($Ch1_{LO} > Ch2_{LO}$)
    - C (2 o'clock) = ($Ch5_{LO} > Ch1_{LO}$) and not ($Ch2_{LO} > Ch5_{LO}$)

  This is the partial jet patch that will be sent on to layer 2. Note that if all three low eta sums are the same (e.g. in an event where nothing happens) then all three comparisons will be false. In this case, sum A, at 10 o'clock, is selected. Use a 2-bit integer to indicate which of the three sums has been selected.
    - 1 = A (10 o'clock)
    - 2 = B (12 o'clock)
    - 3 = C (2 o'clock)

- Step 4: Send to layer 2: the HT.TP bit from each of the 3 jet patches, the 2-bit integer for the combined completed jet patches, the 6 bits of selected partial jet patch sum, its 2-bit ID and the 2 HT bits. The output data format is shown in Table 3.

EMC Layer 2 Algorithm Description

The final piece of this DSM tree is the DSM board at layer 2, EM201, where the BEMC and EEMC data will be combined. The input map to this DSM board is shown in Table 4:

Table 4: Input Map for the EMC Layer 2 DSM Board

Channel	Source	Phi
0	BEMC BC101	10 o'clock
1	BEMC BC102	12 o'clock
2	BEMC BC103	2 o'clock
3	BEMC BC104	4 o'clock
4	BEMC BC105	6 o'clock
5	BEMC BC106	8 o'clock
6	EEMC EE101	4, 6 and 8 o'clock
7	EEMC EE102	10, 12 and 2 o'clock

For the 2018 Run the task of this algorithm is to make the final combinations of HT and back-to-back HT.TP bit combinations.

The layer-2 DSM for the EMC tree therefore performs the following steps:

- RBT File: l1_em201_2018_a.rbt
- User: EM201
- Input:
  6 channels from BEMC:
  - bits 0-8 Unused
  - bit 9 HT.TP threshold bit
  - bits 10-14 HT threshold bits
  - bit 15 Unused

  2 channels from the EEMC:
  - bits 0-1 Unused
  - bit 2 HT.TP-A bit
  - bit 3 HT.TP-B bit
  - bit 4 HT.TP-C bit
  - bits 5-13 Unused
  - bits 14-15 HT threshold bits
- LUT: 1-to-1 mapping
- Registers: None.
- Step 1: Latch Input.
- Step 2: Combine (OR) the HT bits from the two EEMC DSMS.
  Combine (OR) the HT bits from the six BEMC layer 1 DSMS.
  Combine (OR) the HT.TP bits from the BEMC and EEMC for each hour:
  - 4 o'clock = BC104-HT.TP or EE101-HT.TP-A
  - 6 o'clock = BC105-HT.TP or EE101-HT.TP-B
  - Etc…

- Step 3: Delay the HT threshold bits to the 4th step.
  Check for back-to-back combinations of the HT.TP bits
  EMC-UPCtopo = (4 o'clock and 10 o'clock) or
  (6 o'clock and 12 o'clock) or
  (8 o'clock and 2 o'clock)
- Step 4: Latch Output.

Output to TCU:

Bit	Name	Description
Bit 0	BemcHiTwr-th0	Barrel HT0 bit
Bit 1	BemcHiTwr-th1	Barrel HT1 bit
Bit 2	BemcHiTwr-th2	Barrel HT2 bit
Bit 3	BemcHiTwr-th3	Barrel HT3 bit
Bit 4	BemcHiTwr-th4	Barrel HT4 bit
Bit 5	Unused	Unused
Bit 6	Unused	Unused
Bit 7	Unused	Unused
Bit 8	Unused	Unused
Bit 9	EMC-UPCtopo	BEMC+EEMC HT.TP-based UPC topology bit
Bit 10	Unused	Unused
Bit 11	Unused	Unused
Bit 12	Unused	Unused
Bit 13	EemcHiTwr-th0	Endcap HT0 bit
Bit 14	EemcHiTwr-th1	Endcap HT1 bit
Bit 15	Unused	Unused

Output to Scalers:

Bit	Description
Bit 0	Barrel HT0 bit
Bit 1	Barrel HT1 bit
Bit 2	Barrel HT2 bit
Bit 3	Barrel HT3 bit
Bit 4	Barrel HT4 bit
Bit 5:8	Unused
Bit 9	BEMC+EEMC HT.TP-based UPC topology bit
Bit 10:12	Unused
Bit 13	Endcap HT0 bit
Bit 14	Endcap HT1 bit
Bit 15	Unused