# Algorithms for TOF, MTD and PP2PP DSM Tree
# RHIC 2020 Cosmic Ray Running

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Change Log:

| Date | Description |
|---|---|
| January 21, 2016 | First version for the 2016 heavy ion run. The MT101 algorithm has been modified to add in bit meaning "at least one good MTD hit". All the DAQ10k-related logic (test mode and ID selection) has been removed. There are now 2 MTD DSM boards; MT101 and MT102, both of which run the same algorithm. The TF201 algorithm has therefore been modified to combine the muon counts from the two boards. It also passes through all the cosmic bits and the new hit bits. To make room for these extra bits the PP2PP logic was removed since PP2PP is not taking data this run. |
| April 8, 2016 | Second version. The TF201 algorithm has been modified. Two of the MTD Cosmic bits have been combined to make room for a 5$^{th}$ TOF multiplicity threshold. |
| February 2, 2017 | First version for the 2017 proton-proton run. The MTD system has been reduced back to 1 DSM board: MT101. The TF201 algorithm has essentially reverted to the 2015 pp algorithm, so all the PP2PP logic is restored. In order to do this the TOF_UPC bit, which is only used during heavy ion data taking, has been dropped to make room for the MTD hit bit that was added last year. |
| February 22, 2018 | First version for the 2018 cosmic ray running. The TF201 algorithm has reverted to the 2014_a version in which all 6 TOF sector bits are sent to the TCU separately. NOTE: this algorithm contains an old version of the MTD logic that is inconsistent with recent logic changes and no PP2PP logic. |
| February 4, 2019 | First version for the 2019 cosmic ray running. The TF201 algorithm has been modified slightly to pass the MTD single-hit bit through to the TC on a previously unused bit. The duplicate output for the scaler system was also removed because it was never used. |
| November 26, 2019 | First version for the 2020 cosmic ray running. The MT101 and TF201 algorithms have been modified to allow for the introduction of a joint MTD-TOF topology trigger for the GMT. The MT101 algorithm has been simplified by removing the hit, cosmic and timed-cosmic bits and instead just passing 4 good-hit bits on to TF201. The logic to create the MTD hit and cosmic bits has been added to TF201 along with the GMT topology logic. |
| January 14, 2020 | Second version. The TF201 algorithm has been modified to correct a left-right asymmetry problem that had resulted in the wrong TOF hits being used in the GMT trigger logic. |

## Layer 0 DSM Boards: MIX_TF001:006

The TOF layer-0 DSM boards each receive 20 5-bit multiplicity values from the TOF trays. The connections are made such that each layer-0 DSM receives TOF data from one 2-hour pie-slice of the detector. Each 5-bit number is actually a count of how many TOF trays, in a group of 24, were hit. Values greater than 24 are therefore unphysical and are ignored. The values are summed to calculate the total multiplicity. The summing is performed in stages. The result of one of the intermediate stages is 4 numbers, each of which covers ¼ of the 2-hour pie-slice: 2 segments on the East side of the barrel and 2 on the West side. Each of those 4 numbers is compared to two thresholds. The 4 bits associated with the 1st threshold are passed to Layer-1 for use by the Ultra-Peripheral Collisions (UPC) program. The 4 bits associated with the 2nd threshold are passed to the TF202 DSM for use in the DAQ10k readout system. In parallel two signals (the RHIC clock and the run/stop signal) are passed through to the test header. This is being done to help debug a synchronization problem in the TOF layer-0 DSM boards.
NOTE: In order to avoid doing too many sums in parallel, this algorithm takes an extra tick of the RHIC clock, which corresponds to 4 extra ticks of the 4xRHIC clock that is used by the FPGA. This allows many sums to be performed in series, which is easier to implement.

RBT File: mix_tf001_2014_c.rbt

Users: TF001:TF006

Inputs: Ch 0:6 = TOF trays
Ch 7 = Unused

On each DSM channel:
(0:14) 3 5-bit TOF multiplicity values
(15) Unused
NOTE: Ch 6 receives just 2 input multiplicity values so it uses only bits 0:9

LUT: 1-to-1. Noisy, dead and non-instrumented channels are also zeroed out here

Registers:
R0: TOF_upc_th (8)
R1: TOF_DAQ10k_th (8)

Action

1st Latch inputs

2nd Zero out any channel with a value greater than 24

3rd Sum TOF channels 0:2, 3:4, 5:7, 8:9, 10:12, 13:14, 15:17 and 18:19

4th Combine these sums in pairs to make the sums of channels 0:4, 5:9, 10:14 and 15:19.
NOTE: Each of these sums covers 1 unit in $\eta$ and $\pi/6$ (i.e. 1/12 of the barrel = 1 hour) in $\phi$. The cabling of the TOF data into the DSM boards is such that the ordering is the same for all 6 TOF layer-0 DSM boards. WHEN VIEWED FROM THE EAST:

- Sum 0:4 = West, low hour
- Sum 5:9 = West, high hour
- Sum 10:14 = East, low hour

- Sum 15:19 = East, high hour

5th Combine these sums in pairs to make the sums of channels 0:9 and 10:19.
Compare each of the 4 sums to the UPC threshold in register 0. The logic looks for sum(channels 0:4) > reg0, etc…
Compare each of the 4 sums to the DAQ10k threshold in register 1. The logic looks for sum(channel 0:4) > reg1, etc…

6th Combine these two sums to make the final sums of channels 0:19.
Also delay the UPC and DAQ10k threshold bits to the 8th step.

7th Delay the final sum

8th Latch Outputs

Output to TF101:
(0:9) TOF multiplicity
(10:13) UPC threshold bits
(14:15) Unused

Output to TF202:
(16:19) DAQ10k threshold bits
(20:31) Unused

Output to Test Header:
(0) Run/Stop signal from Operation Control FPGA
(2:14) Unused
(15) RHIC clock

## 1. Layer 1 DSM Board: MIX_TF101

The TOF layer-1 DSM board receives a 10-bit multiplicity value and 4 UPC threshold bits from each of the six TOF layer-0 DSM boards. Each input multiplicity is compared to a threshold. In parallel with this, the values are also summed to calculate the total multiplicity. For the UPC program, the 24 input bits are masked so the UPC group can constrain which topologies they will trigger on. The masked bits are then searched to look for interesting combinations. The cabling is such that:

TF001 covers sectors that start at 9 o'clock and 10 o'clock when viewed from the East
TF002 covers sectors that start at 11 o'clock and 12 o'clock
TF003 covers sectors that start at 1 o'clock and 2 o'clock
TF004 covers sectors that start at 3 o'clock and 4 o'clock
TF005 covers sectors that start at 5 o'clock and 6 o'clock
TF006 covers sectors that start at 7 o'clock and 8 o'clock

NOTE: In order to avoid doing too many sums in parallel, this algorithm takes an extra tick of the RHIC clock, which corresponds to 4 extra ticks of the 4xRHIC clock that is used by the FPGA. This allows many sums to be performed in series, which is easier to implement.

RBT File: mix_tf101_2014_b.rbt

Users: TF101

Inputs: Ch 0:5 = TF001:TF006
Ch 6:7 = Unused

On each DSM channel:
(0:9) TOF multiplicity
(10:13) UPC threshold bits
(14:15) Unused

LUT: 1-to-1

Registers:
R0: TOF_sector_th (10)
R1: TOF_upc_East_mask (12)
R2: TOF_upc_West_mask (12)

Action

1st Latch inputs

2nd Sum channels 0:1, 2:3 and 4:5
Compare each of the 6 input multiplicity values to the threshold specified in register 0. Mask out the UPC bits using the values masks specified in register 1 (East) and register 2 (West). A "1" in the mask enables a UPC bit, "0" will disable that bit. BOTH masks are coded such that:
bit(0) enables/disables the sector that starts at 12 o'clock AS VIEWED FROM THE EAST
bit(1) enables/disables the sector that starts at 1 o'clock AS VIEWED FROM THE EAST
…
bit(11) enables/disables the sector that starts at 11 o'clock AS VIEWED FROM THE EAST

3rd Combine the first two sums to make the sums of channels 0:3.
Delay the sum of channels 4 and 5 to the 4th step.
Delay the 6 threshold bits to the 8th step.
Combine (OR) the East and West UPC bits for each $\phi$ value and then look for all possible combinations separated by 4 hours, i.e.
1 o'clock = East 1 o'clock OR West 1 o'clock
2 o'clock = East 2 o'clock OR West 2 o'clock
…
12 o'clock = East 12 o'clock OR West 12 o'clock

TOF_UPC = 12 o'clock AND 4 o'clock OR
1 o'clock AND 5 o'clock OR
…
11 o'clock AND 3 o'clock

4th Combine the two remaining sums to make the final total multiplicity sum of channels 0:5.
Delay the TOF_UPC bit to the 8th step.

5th Delay the final sum to the 8th step.

6/7th No logic

8th Latch Outputs

Output to TF201:

| | |
|---|---|
| (0:12) | TOF total multiplicity |
| (13:15) | Unused |
| (16:21) | 6 sector threshold bits |
| (22) | TOF_UPC bit |
| (23:31) | Unused |

## 2. Layer 0 QT Board: MXQ_MT001:008

All four MTD QT boards in the MXQ crate are using the same algorithm. That algorithm forms TAC pair sums and then finds the two largest sums to pass on to the DSM tree. Please see the documentation provided by Chris Perkins for a detailed description of this algorithm at http://www.star.bnl.gov/public/trg/TSL/Software/qt_v6_c_doc.pdf

## 3. Layer 0 QT Board: MXQ_VP003:004

The two VPD QT boards in the MXQ crate use the STAR-standard fastest-TAC algorithm. The algorithm produces the TAC value of the fastest good hit and the sum of ADC values from all good hits. A slew correction is applied to the TAC values before good hits are selected. Please see the documentation provided by Chris Perkins for a detailed description of the algorithm at http://www.star.bnl.gov/public/trg/TSL/Software/qt_v6_d_doc.pdf

## 4. Layer 1 DSM Board: MIX_MT101

The MT101 DSM receives its data through a TDSMI, so there are 10 12-bit input channels. The algorithm receives the 2 best TAC sums from each of 4 MTD QT boards. It also receives the fastest (largest) TAC values from the QT boards covering the East and West sides of the VPD (MXQ_VP003/4). The cables carrying the VPD ADC sums are not connected to MT101 so that data is not received. There are two separate logic streams flowing through the algorithm:
**Muons**: The VPD TAC sum is calculated. Then the algorithm calculates the difference between each MTD TAC sum and that VPD TAC sum. All 8 TAC differences are checked to determine if they are inside a window. Those that are inside the window are counted, and the count is sent on to TF201.
**Cosmic Rays**: A hit bit is set for the 1st (best) MTD TAC sum received from each QT board if it is non-zero. The resulting 4 bits are sent to TF201 for use in MTD test triggers and also in the GMT topology trigger. The 2nd best TAC sum received from each QT board is ignored by this logic stream.

NOTE: This algorithm takes an extra tick of the RHIC clock to implement all the logic.

RBT File: mix_mt101_2020_a.rbt

Users: MT101

Inputs: Ch0:1 = MT001 = MTD
Ch2:3 = MT002 = MTD

Ch4:5 = MT003 = MTD
Ch6:7 = MT004 = MTD
Ch8 = VP003 = VPD East
Ch9 = VP004 = VPD West

From the MTD QT boards:
Bits 0:9 = Best MTDE+MTDW TAC sum (value=0 means not enough good hits)
Bits 10:11 = Unused
Bits 12:21 = 2nd best MTDE+MTDW TAC sum (value=0 means not enough good hits)
Bits 22:23 = Unused

From VP003/4 QT boards:
Bits 0:11 = Max TAC (value=0 implies no good hits)

LUT: 1:1

Registers:
R0: MTD_VPD_TACdiff_Min (11)
R1: MTD_VPD_TACdiff_Max (11)
R2: MTD_InputCh_Bitmask (8)
Bit x = 0 turns off ChX, Bit x = 1 turn on ChX

Action:

1st Latch input

2nd Define Good_VPD_E = VPDE-TAC > 0
Define Good_VPD_W = VPDW-TAC > 0
Calculate 13-bit VPD-sum = VPDE TAC + VPDW TAC
Truncate VPD-sum to 10-bits by dropping 3 LSB
For each MTD ChX:
Zero out MTD-TAC-X if R2(x) = 0

3rd Define Good_VPD = Good_VPD_E and Good_VPD_W.
For each MTD ChX:
Define: Good_ChX = MTD-TAC-X > 0
Calculate: MTD-VPD-TACdiffX = 1024 + MTD-TAC-X – VPD-sum

4th Make a separate copy the Good_ChX bits from Ch0, 2, 4 and 6, i.e. the best TAC sum from each QT board.
For each MTD ChX:
Compare the TACdiffX value to the min and max values specified in R0 and R1
TACdiffX-min = MTD-VPD-TACdiffX > R0
TACdiffX-max = MTD-VPD-TACdiffX < R1
Zero out TACdiffX-min/max if EITHER Good_VPD or Good_ChX is FALSE.
Combine the min and max values to determine if the TAC difference is inside the window:
TACdiff-in-window-X = TACdiffX-min and TACdiffX-max

5th Count how many TACdiff-in-window bits are true = num-muons

6th Delay all the results to the 7th step

7th Delay all the results to the 8th step

8th Latch output

Output to TF201:

(0:3) num_muons
(4:11) "MTD-VPD TAC difference in window" bits
(12) MT001 good-hit bit
(13) MT002 good-hit bit
(14) MT003 good-hit bit
(15) MT004 good-hit bit

## 5. Layer 0 QT Board: MXQ_PP001

Please see the documentation provided by Chris Perkins for a description of the algorithm at http://www.star.bnl.gov/public/trg/TSL/Software/qt_v5_2_doc.pdf

## 6. Layer 1 PP2PP DSM Board: MIX_PP101

The PP101 DSM board receives 16 "good hit" bits from the PP001 QT board. Those bits are combined to make "good detector" bits, which are themselves combined to make the trigger and scaler bits. All the bits are passed on to TF201, which separates the trigger bits from the scaler bits and sends them to the appropriate place. A mask register is available to turn each "good hit" bit on or off in case of problems.

RBT File: mix_pp101_2015_a.rbt

Users: PP101

Inputs Ch 0 = PP001
Ch 1:7 = Unused

From: The PP2PP QT board

(0) E2U1 = Roman Pot East-2 (Back) Up 1
(1) E2U2 = Roman Pot East-2 (Back) Up 2
(2) E2D1 = Roman Pot East-2 (Back) Down 1
(3) E2D2 = Roman Pot East-2 (Back) Down 2
(4) W2U1 = Roman Pot West-2 (Back) Up 1
(5) W2U2 = Roman Pot West-2 (Back) Up 2
(6) W2D1 = Roman Pot West-2 (Back) Down 1
(7) W2D2 = Roman Pot West-2 (Back) Down 2
(8) E1D1 = Roman Pot East-1 (Front) Down 1
(9) E1D2 = Roman Pot East-1 (Front) Down 2
(10) E1U1 = Roman Pot East-1 (Front) Up 1
(11) E1U2 = Roman Pot East-1 (Front) Up 2
(12) W1D1 = Roman Pot West-1 (Front) Down 1
(13) W1D2 = Roman Pot West-1 (Front) Down 2
(14) W1U1 = Roman Pot West-1 (Front) Up 1
(15) W1U2 = Roman Pot West-1 (Front) Up 2

LUT: 1-to-1

Registers:

R0: PP2PP_RPmask (16)

NOTE: The bits are arranged in the SAME ORDER as the input data coming from PP001
Bit 0 = E2U1 on(1) or off (0)
Bit 1 = E2U2 on(1) or off (0)
…
Bit 15 = W1U2 on(1) or off (0)

Action

1st Latch inputs

2nd Combine the 2 hits from the same counter, and then combine the 2 counters on each side, to make the detector bits. Mask each hit with Reg0 before it is used.

E2U = (E2U1 and Reg0(0)) or (E2U2 and Reg0(1))
E2D = (E2D1 and Reg0(2)) or (E2D2 and Reg0(3))
W2U = (W2U1 and Reg0(4)) or (W2U2 and Reg0(5))
W2D = (W2D1 and Reg0(6)) or (W2D2 and Reg0(7))
Same for E1D, E1U, W1D, W1U

EU = E1U or E2U
ED = E1D or E2D
WU = W1U or W2U
WD = W1D or W2D

3rd Delay a copy of the detector bits (EU, ED, WU and WD) to the 4th step.
Combine the detector bits to make the trigger bits

EA (Elastic Trigger A) = EU and WD
EB (Elastic Trigger B) = ED and WU
IU (Inelastic Trigger Up) = EU and WU
ID (Inelastic Trigger Down) = ED and WD

ET (Elastic Trigger) = EA or EB
IT (Inelastic Trigger) = IU or ID
EOR (East OR) = EU or ED
WOR (West OR) = WU or WD

4th Latch Outputs

Output to TF201:

(0:3) ET, IT, EOR, WOR
(4:7) EU, ED, WU, WD
(8:15) Unused

## 7. Layer 2 TOF DSM Board: L1-TF201

All the information from the TOF, MTD and PP2PP detectors is brought into the TOF layer 2 DSM. The TOF_UPC topology bit and the TOF sector threshold bits are passed through to the TCU. The TOF multiplicity is compared to five thresholds. The MTD good-hit bits are counted. The MTD-Hit bit is set if

the count is at least 1 and the MTD-Cosmic bit is set if the count is at least 2. The TOF sector threshold bits and the MTD good-hit bits are also combined to creator the 5 GMT topology triggers.

The GMT modules replace TOF slats in trays 8, 23, 93 and 108. This means the GMT modules are located at 2 o'clock and 5 o'clock when viewed from the West, i.e. 10 o'clock and 7 o'clock when viewed from the East. Those TOF trays feed into TF001 (trays 8 and 108) and TF006 (trays 23 and 93). The aim of the GMT triggers is to select tracks that traverse the TPC and hit one of the GMT modules. These tracks would leave 2 hits in the MTD, on opposite sides of the TPC barrel, but only one hit in the TOF barrel. That TOF hit would be on the far side of the TPC away from the hit GMT module. There are 5 possible combinations of MTD and TOF sector hits that correspond to these conditions and all 5 are included here. The resulting 5 trigger bits are OR'ed together to create the final GMT bit, with a register to turn each of the 5 components on/off in the OR. The algorithm ignores the MTD muon count and the PP2PP data.

RBT File: l1_tf201_2020_b.rbt

Users: TF201

Inputs: Ch 0 = MT101
Ch 1 = Unused
Ch 2:3 = TF101
Ch 4 = PP101 (unused in this algorithm)
Ch 5:7 = Unused

From MTD Layer 1 DSM - MT101 on Ch. 0
(0:11) Unused
(12) MT001 good-hit bit
(13) MT002 good-hit bit
(14) MT003 good-hit bit
(15) MT004 good-hit bit

From TOF Layer 1 DSM - TF101 on Ch. 2
(0:12) TOF total multiplicity
(13:15) Unused

From TOF Layer 1 DSM - TF101 on Ch. 3
(0:5) TOF sector threshold bits
Bit 0 = TF001
Bit 1 = TF002
…
Bit 5 = TF006
(6) TOF UPC topology bit
(7:15) Unused

LUT: 1-to-1

Registers:
R0: TOF_mult0 (13)
R1: TOF_mult1 (13)
R2: TOF_mult2 (13)
R3: TOF_mult3 (13)

R4: TOF_mult4 (13)
R5: GMT_onoff (5)

Action

1st Latch inputs

2nd Delay the TOF_UPC topology bit and the TOF sector threshold bits to the 4th step.
Compare the TOF total multiplicity to the thresholds specified in registers 0 to 4.
Count the MTD good-hit bits
Combine the MTD good-hit bits and the TOF sector threshold bits for GMT:
GMT-0 = MT001 and MT003 and (TF003 or TF004 or TF005 or TF006)
GMT-1 = MT001 and MT002 and TF003
GMT-2 = MT002 and MT004 and (TF002 or TF003)
GMT-3 = MT001 and MT004 and (TF001 or TF002)
GMT-4 = MT003 and MT004 and TF004

3rd Delay the TOF multiplicity bits to the 4th step.
Set the MTD-Hit bit to 1 if the good-hit count > 0
Set the MTD-Cosmic bit to 1 if the good-hit count > 1
Combine (OR) the 5 GMT trigger bits using the bits in R5 to turn each trigger bit on (1) or off (0):
GMT = (GMT-0 and R5(0)) or (GMT-1 and R5(1)) or etc…

4th Latch Outputs

Output to TCU:

| Bit | Name | Description |
|---|---|---|
| Bit 0 | GMT | MTD-TOF topology trigger for GMT |
| Bit 1 | Unused | Unused |
| Bit 2 | MTD-Hit | At least 1 good hit in the MTD |
| Bit 3 | TOF_UPC | TOF UPC topology bit |
| Bit 4 | TOFmult0 | TOF total multiplicity > th0 |
| Bit 5 | TOFmult1 | TOF total multiplicity > th1 |
| Bit 6 | TOFmult2 | TOF total multiplicity > th2 |
| Bit 7 | TOFmult3 | TOF total multiplicity > th3 |
| Bit 8 | TOFmult4 | TOF total multiplicity > th4 |
| Bit 9 | TOFsector0 | TOF sector 0 multiplicity > th |
| Bit 10 | TOFsector1 | TOF sector 1 multiplicity > th |
| Bit 11 | TOFsector2 | TOF sector 2 multiplicity > th |
| Bit 12 | TOFsector3 | TOF sector 3 multiplicity > th |
| Bit 13 | TOFsector4 | TOF sector 4 multiplicity > th |
| Bit 14 | TOFsector5 | TOF sector 5 multiplicity > th |
| Bit 15 | MTD-Cosmic | At least 2 good hits in the MTD |