DSM Algorithms for the DAQ10k Readout

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Change Log:

Date	Description
February 27, 2014	First version describing all the DAQ10k-related algorithms.
March 21, 2014	No logic changes. In MT201 the order of the best and 2nd best channels was reversed on the cable coming from MT101. The documentation has been fixed.
March 27, 2014	No logic changes. The name of a register in DQ301 was updated to include the "DAQ10k" tag to make it more obvious to STAR users what it is for.
April 3, 2014	No logic changes. There was a mistake in the "MTD Sector" column of Table 4 on page 7. This has been fixed.
April 18, 2014	First version of the TF202 algorithm has been created.

The DAQ10k readout scheme aims to reduce the time taken to read out the STAR TPC for some events by only reading out those sectors that contain tracks from interesting particles. The selection of interesting particles is done using the fast trigger detectors: BEMC, MTD and TOF. Each of those 3 detectors forms a barrel that surrounds the TPC. A subset of DSM boards translates the information from each trigger detector into a list of TPC sectors. A final DSM board then selects the appropriate list depending on which type of trigger was issued. This scheme is shown in Figure 1.

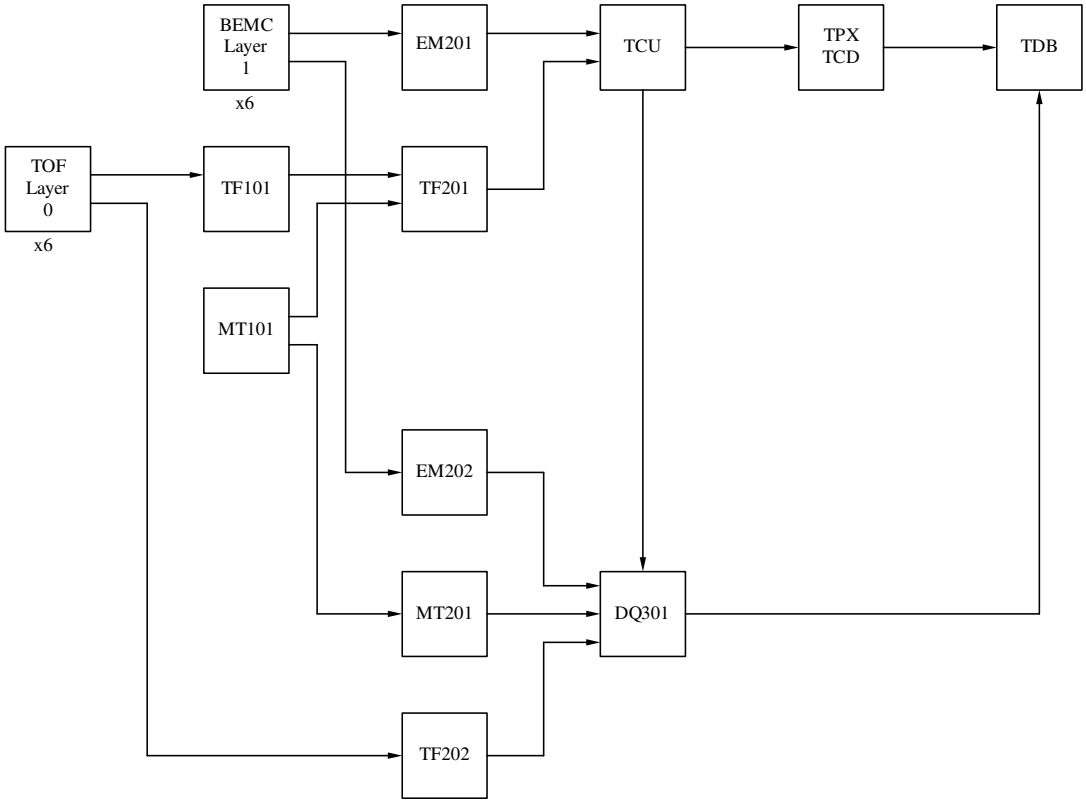

Figure 1: Detail of the DSM Tree showing the DAQ10k-related Connections

The algorithms for the purely DAQ10k-related DSM boards (EM202, MT201, TF202 and DQ301) are described here. A brief description of the DAQ10k-related TCU code is also included.

1. EMC DAQ10k DSM: EM202

This DSM board receives the DAQ10k-selected BEMC HT bits via the second output cable of the six BEMC layer-1 DSM boards. It uses them to create a 24-bit mask showing which TPC sectors the particles travelled through before they hit the BEMC towers.

The association between the layer-0 BEMC DSM boards which create the HT bits and the TPC sectors is shown in Figures 2 and 3. The inner part of each diagram shows the TPC sectors. The next ring out shows the BEMC modules and the outer layer shows how those modules connect to the BEMC layer-0 DSM boards.

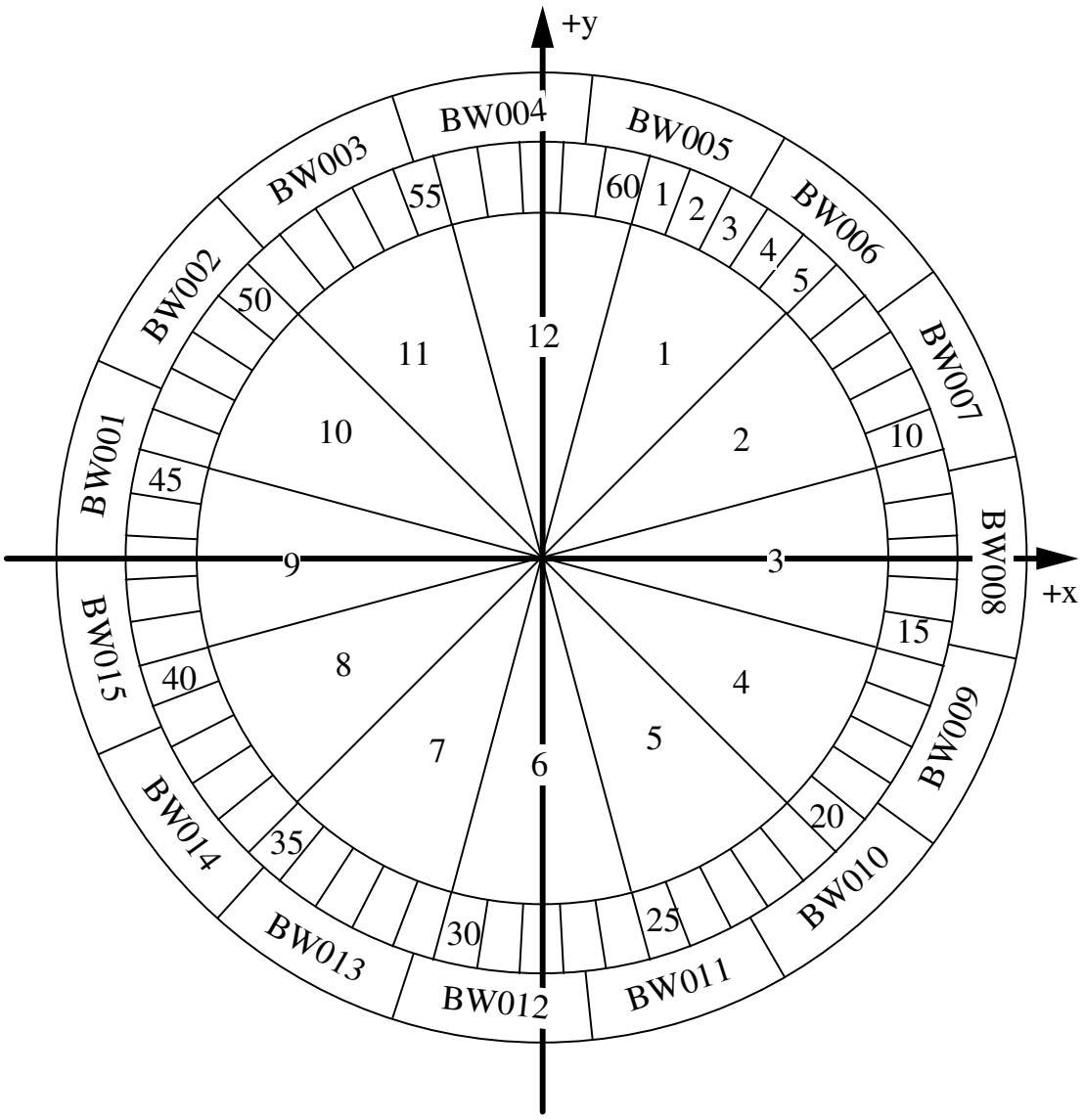

Figure 2: West End of the TPC/BEMC Barrel seen from outside the TPC looking back (East) towards the center.

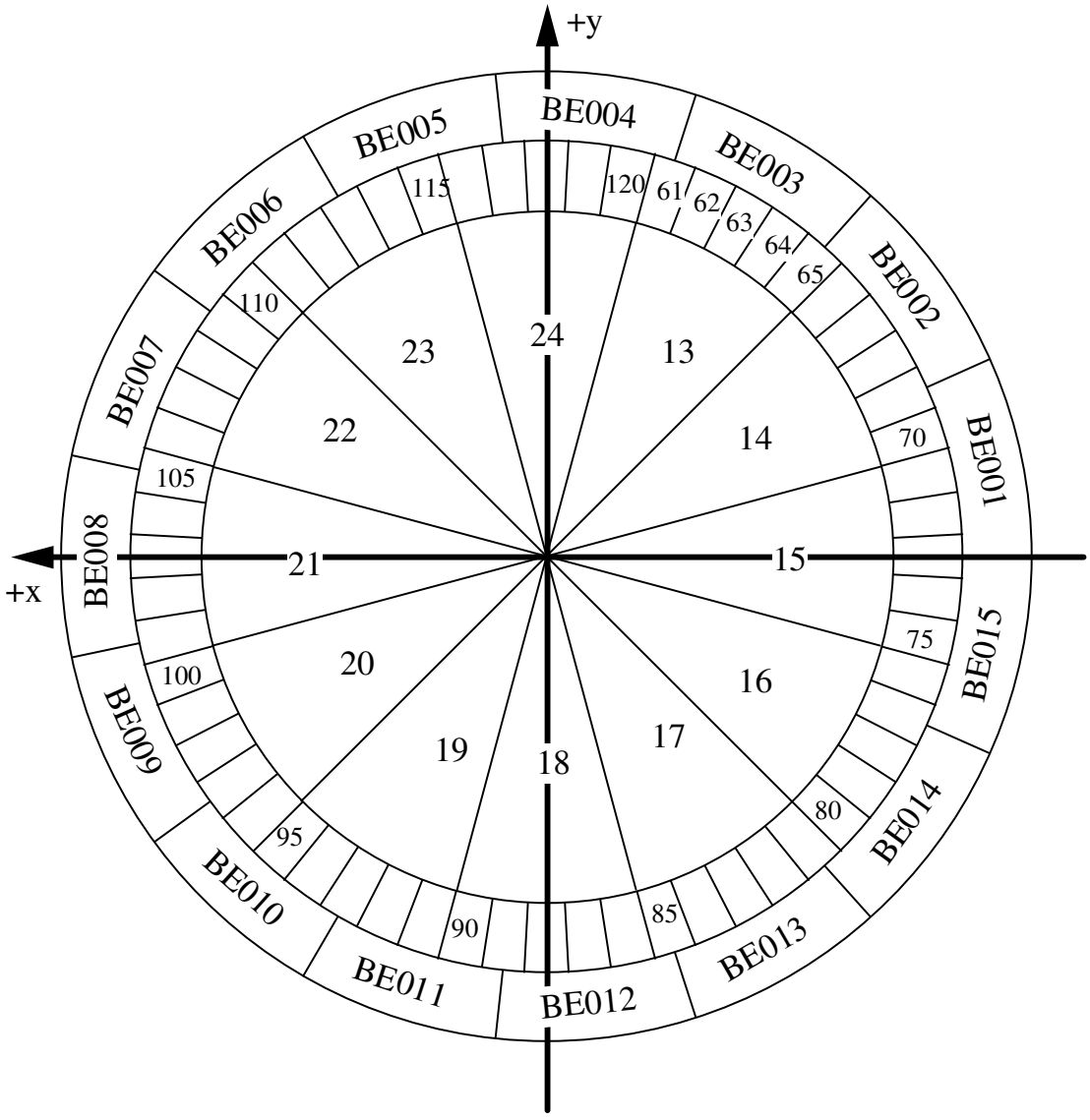

Figure 3: East End of the TPC/BEMC barrel seen from outside the TPC looking back (West) towards the center.

The 6 DAQ10k HT bits, selected by each of the six BEMC layer-1 DSM boards and passed on to this EM202 DSM board, describe which layer-0 DSM boards received HT values over the selected threshold. The input map is shown in Table 1. The column "Layer-0 DSM boards: bits(0:5)" shows the layer-0 DSM boards in order, i.e. of the six HT bits that come to EM202 from BC101 HT(0) comes from BE001, HT(1) comes from BW001, etc… The six double-output layer-0 DSM boards are obviously BE/W003, 8 and 13. Each of these boards sends two sets of data to the layer-1 DSM boards, which then pass the selected HT bits on to EM202. So BE003, for example, shows up twice in Table 1.

Table 1: Input Map for the EM202 DSM Board

Channel	Source	Phi	Layer-0 DSM boards: bits(0:5)
0	BC101	10 o'clock	BE001, BW001, BE002, BW002, BE003a, BW003a
1	BC102	12 o'clock	BE003b, BW003b, BE004, BW004, BE005, BW005
2	BC103	2 o'clock	BE006, BW006, BE007, BW007, BE008a, BW008a
3	BC104	4 o'clock	BE008b, BW008b, BE009, BW009, BE010, BW010
4	BC105	6 o'clock	BE011, BW011, BE012, BW012, BE013a, BW013a
5	BC106	8 o'clock	BE013b, BW013b, BE014, BW014, BE015, BW015
6	Unused		
7	Unused		

An algorithm has been created that combines this information with the connections shown in Figures 2 and 3 to create the sector readout mask for the TPC. This map is shown in Table 2.

Table 2: TPC Sector-Readout Map

TPC Sector	Layer-0 DSM boards: bits(0:5)
1	BW005 or BW006
2	BW006 or BW007
3	BW007 or BW008a or BW008b or BW009
4	BW009 or BW010
5	BW010 or BW011
6	BW011 or BW012
7	BW012 or BW013a or BW013b or BW014
8	BW014 or BW015
9	BE015 or BW001
10	BW001 or BW002
11	BW002 or BW003a or BW003b or BW004
12	BW004 or BW005
13	BE004 or BE003a or BE003b or BE002
14	BE002 or BE001
15	BE001 or BE015
16	BE015 or BE014
17	BE014 or BE013a or BE013b or BE012
18	BE012 or BE011
19	BE011 or BE010
20	BE010 or BE009
21	BE009 or BE008a or BE008b or BE007
22	BE007 or BE006
23	BE006 or BE005
24	BE005 or BE004

In addition the algorithm includes two test modes to allow the user to generate pre-determined TPC sector-readout masks for debugging purposes. The EM202 algorithm therefore performs the following steps:

RBT File: l1_em202_2012_a.rbt

User: EM202

Input: 6 channels from the BEMC layer-1 DSM boards, as shown in Table 1.

LUT: 1-to-1 mapping

Registers:

R0: EMC-DAQ10k-Mode (2 bits)
- 0 => Data-based TPC sector-readout mask
- 1 => Fixed test sector-readout mask
- 2 => Variable test sector-readout mask

R1: EMC-DAQ10k-Test-Pattern-12LSB (12)
R2: EMC-DAQ10k-Test-Pattern-12MSB (12)
R3: EMC-DAQ10k-Test-Rate-12LSB (12)
R4: EMC-DAQ10k-Test-Rate-12MSB (12)

Action:

1st Latch input.

2nd Combine the received HT bits using the equations shown in Table 2 to create the 24-bit data-based TPC sector-readout mask.
Also create the test sector-readout mask.
When the DSM is not in RUN mode an initial test mask is created by concatenating the patterns loaded into R1 and R2. Also, a 24-bit prescale counter is initialized by combining the values in registers R3 and R4.
Once the DSM board is in run mode the prescale counter decrements by 1 every tick of the RHIC clock. When the counter reaches 1 it is reset to the original value from R3 and R4.
If the counter value is 1 then:
If R0 = 1: test sector-readout mask is set to its initial value
If R0 = 2: test sector-readout mask is shifted up by one bit, and the MSB is reloaded as the new LSB.
Else (i.e. counter value has not yet reached 1)
Set test sector-readout mask to zero.

3rd Select either the data-based readout mask, or the test sector-readout mask based on the value of R0

4th Latch output. The output format is shown in Table 3.

Table 3: Output of Layer 2 EM202 DSM Board

Bits	Data
0:11	EMC-based TPC Readout Mask: Sectors 1:12
12:15	Unused
16:27	EMC-based TPC Readout mask: Sectors 13:24
28:31	Unused

2. MTD DAQ10k DSM: MT201

This DSM board receives the ID information of the two best MTD hits from the MT101 DSM. It uses them to create a 24-bit mask showing which TPC sectors the particles travelled through before they hit the MTD. The association between the DSM channel numbers, the MTD ID value and the TPC sectors is shown below.

Table 4: MTD Tray to TPC Sector Conversion

QT Board	DSM Channel number	MTD ID value	MTD sector	TPC sector
MT001	1, 2	0	5	21, 22
		1	11	2, 3
		2	6	23, 24
		3	12	1, 12
MT002	3, 4	0	1	13, 14
		1	7	10, 11
		2	6	23, 24
		3	12	1, 12
MT003	5, 6	0	2	15, 16
		1	8	8, 9
		2	3	17, 18
		3	9	6, 7
MT004	7, 8	0	4	19, 20
		1	10	4, 5
		2	3	17, 18
		3	9	6, 7

RBT File: mix_mt201_2014_a.rbt

Users: MT201

Inputs: Ch 0 = MT101
Ch 1:7 = Unused

From MT101
(0-3) DSM Channel number (1:8) of 2nd best good MTD value
(4:5) MTD ID value from that channel
(6:9) DSM Channel number (1:8) of best good MTD value
(10:11) MTD ID value from that channel

LUT: 1-to-1

Registers:
None

Action

1st Latch input

2nd Convert the DSM Channel number and MTD ID value into a 16-bit mask indicating which two MTD sectors were selected, as shown in Table 4

.

3rd Convert the 16-bit MTD sector mask to a 24-bit TPC sector-readout mask using the mapping shown in the last two columns of Table 4.

4th Latch Output. The output format is shown in Table 5.

Table 5: Output of Layer 2 MT201 DSM Board

Bits	Data
0:11	MTD-based TPC Readout Mask: Sectors 1:12
12:15	Unused
16:27	MTD-based TPC Readout mask: Sectors 13:24
28:31	Unused

3. TOF DAQ10k DSM: TF202

This DSM board receives the DAQ10k-related TOF pixel bits via the second output cable of the six TOF layer-0 DSM boards. It uses them to create a 24-bit mask showing which TPC sectors the particles travelled through before they hit the TOF trays.

The association between the layer-0 TOF DSM boards which create the pixel bits and the TPC sectors is shown in Figures 4 and 5. The inner part of each diagram shows the TPC sectors. The outer ring shows how those sectors relate to the TOF layer-0 DSM boards. The dashed lines show how each TOF layer-0 DSM board splits its TOF trays into the 4 pixels; a and b at the West end, c and d at the East end.

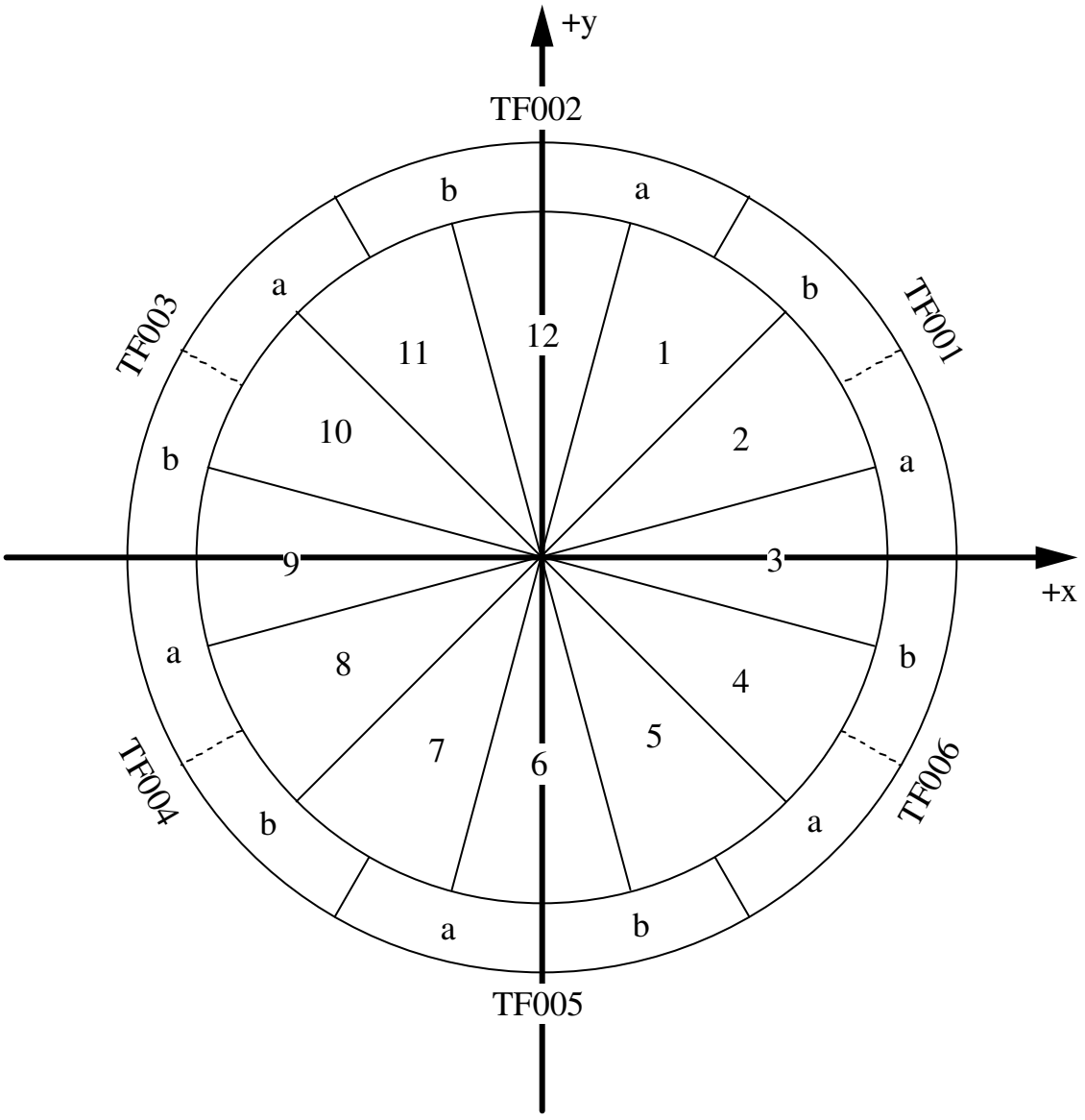

Figure 4: West End of the TPC and TOF seen from outside the TPC looking back (East) towards the center.

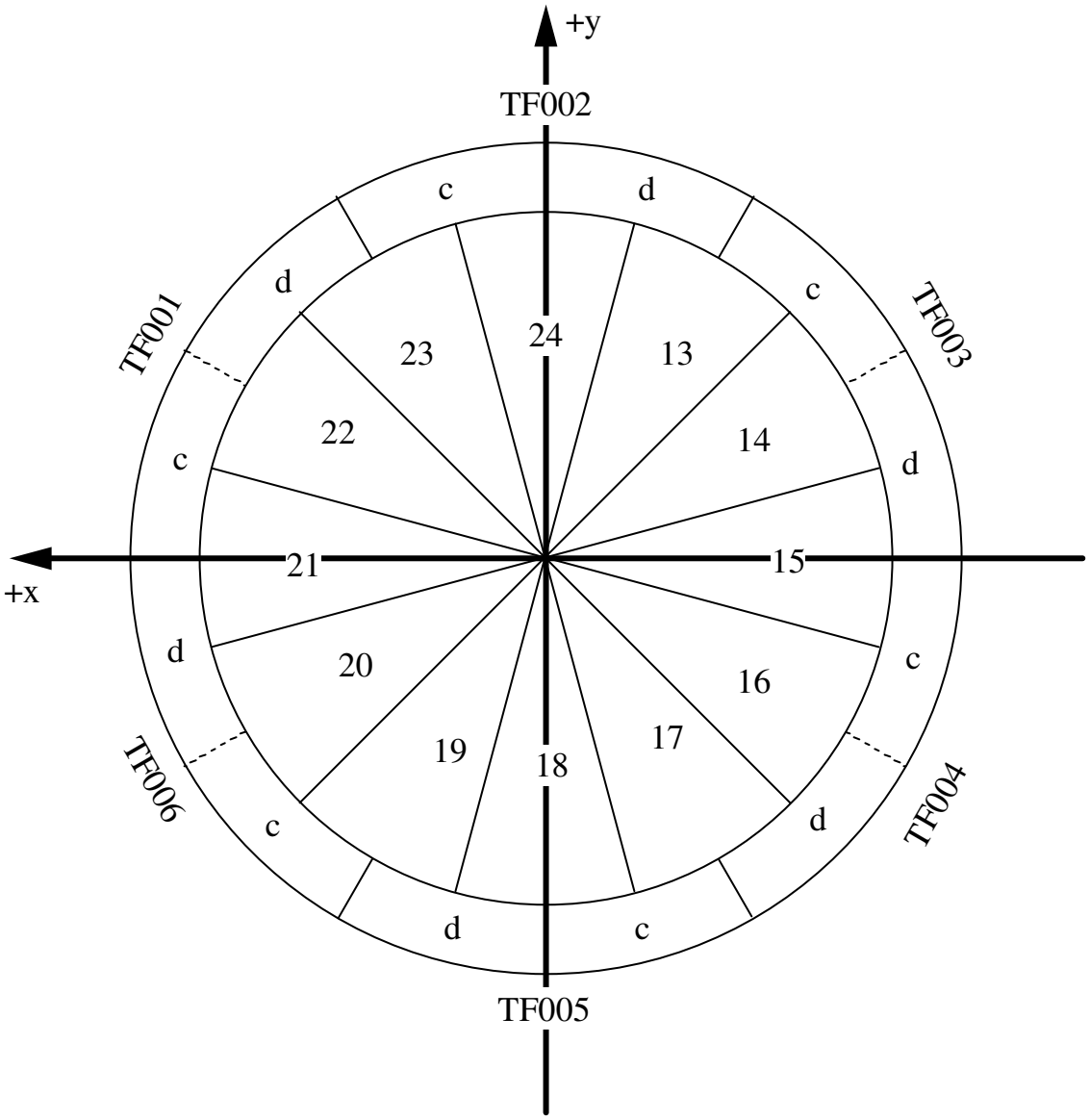

Figure 5: East End of the TPC and TOF seen from outside the TPC looking back (West) towards the center.

The DAQ10k pixel bits, created by each of the six TOF layer-0 DSM boards and passed on to this TF202 DSM board, describe which pixels had a total multiplicity that exceeded a threshold. The routing of the bits has been set up in such a way that ordering of the pixel bits is always the same. The input map is shown in Table 6. The column "Pixels: bits(0:3)" shows the pixels in order, i.e. of the four pixel bits that come to TF202 from TF001 bit(0) comes from pixel "a", bit(1) comes from pixel "b", etc…

Table 6: Input Map for the TF202 DSM Board

Channel	Source	Pixels: bits(0:3)
0	TF001	a, b, c, d
1	TF002	a, b, c, d
2	TF003	a, b, c, d
3	TF004	a, b, c, d
4	TF005	a, b, c, d
5	TF006	a, b, c, d
6	Unused	
7	Unused	

An algorithm has been created that combines this information with the connections shown in Figures 4 and 5 to create the sector readout mask for the TPC. This map is shown in Table 7.

Table 7: TPC Sector-Readout Map

TPC Sector	Layer-0 DSM boards: pixels(a:d)
1	TF001(b) or TF002(a)
2	TF001(a) or TF001(b)
3	TF006(b) or TF001(a)
4	TF006(a) or TF006(b)
5	TF005(b) or TF006(a)
6	TF005(a) or TF005(b)
7	TF004(b) or TF005(a)
8	TF004(a) or TF004(b)
9	TF003(b) or TF004(a)
10	TF003(a) or TF003(b)
11	TF002(b) or TF003(a)
12	TF002(a) or TF002(b)
13	TF002(d) or TF003(c)
14	TF003(c) or TF003(d)
15	TF003(d) or TF004(c)
16	TF004(c) or TF004(d)
17	TF004(d) or TF005(c)
18	TF005(c) or TF005(d)
19	TF005(d) or TF006(c)
20	TF006(c) or TF006(d)
21	TF006(d) or TF001(c)
22	TF001(c) or TF001(d)
23	TF001(d) or TF002(c)
24	TF002(c) or TF002(d)

The TF202 algorithm therefore performs the following steps:

RBT File: mix_tf202_2014_a.rbt

User: TF202

Input: 6 channels from the TOF layer-0 DSM boards, as shown in Table 6.

LUT: 1-to-1 mapping

Registers:
None

Action:

1st Latch input.

2nd Combine the received pixel bits using the equations shown in Table 7 to create the 24-bit data-based TPC sector-readout mask.

3rd Delay that mask to the 4th step.

4th Latch output. The output format is shown in Table 8.

Table 8: Output of Layer 2 TF202 DSM Board

Bits	Data
0:11	TOF-based TPC Readout Mask: Sectors 1:12
12:15	Unused
16:27	TOF-based TPC Readout mask: Sectors 13:24
28:31	Unused

4. TCU DAQ10k-related Logic

The DAQ10k-related logic in the Trigger Control Unit is very simple:

- The TCU has 64 triggers operating in parallel
- For each trigger the user can define a DAQ10k command word. The word is actually a 4-bit list:
    - Bit 0 = use the EMC information to make the TPC readout mask.
    - Bit 1 = use the MTD information to make the TPC readout mask.
    - Bit 2 = use the TOF information to make the TPC readout mask.
    - Bit 3 = generate a mask to readout all TPC sectors..
- For every RHIC clock tick the TCU makes an OR of the DAQ10k command words of all the satisfied triggers
- The combined word is sent to the DQ301 DSM

5. Final DSM Board: DQ301

This algorithm is used to generate the bitmask that is used by the TPC gated-grid driver to determine which TPC sectors are read out. Up to 3 incoming bitmasks are available. Currently they are provided by the EMC, MTD and TOF branches of the DSM tree. The final mask that is sent to the gated-grid driver is generated making an OR of whichever of the incoming masks the user selects. There are two ways for the user to define the selection:

a) The algorithm receives a 4-bit word from the TCU that can be used to change the selection on an event-by-event basis.
b) There is a 4-bit register that can override the TCU input and allow the user to specify that a particular incoming mask should always be selected.

If the most significant bit of the 4-bit register is on then the DQ301 algorithm automatically generates an output bitmask that has all 24 TPC sectors turned on.

RBT File: l1_dq301_2014_a.rbt

Users: DQ301

Inputs: Ch 0/1 = EM202
Ch 2/3 = MT201
Ch 4/5 = TF202
Ch 6/7 = Unused
Ch 8 = TCU
Ch 9 = Unused

From EM202, MT201 and TF202
(0-23) 24-bit TPC sector readout mask

From TCU
(0) Select Ch 0/1 (EM202)
(1) Select Ch 2/3 (MT201)
(2) Select Ch 4/5 (TF202)
(3) Generate mask to readout all TPC sectors

LUT: 1-to-1

Registers:

R0: DAQ10k_TCU_select_enable (1 bit)

0 = Ignore TCU input, 1 = Use TCU input

R1: DAQ10k_Mask_Select (4 bits)

The 4 bits have the same definition as the 4 bits from the TCU

Action

1st Latch incoming bitmasks

2nd If R0 = 1then

switches = data from TCU

else

switches = data from R1

For each of the 3 data inputs (X = 0:2 = EMC, MTD and TOF):

Zero out the input bitmask if switches(X) = 0

If switches(3) = 1 then

generate a 24-bit mask with all bits on

else

generate a 24-bit mask with all bits off.

3rd Combine (OR) all 4 masks, including the internally generated one:

Output = mask(0) or mask(1) or mask(2) or generated mask(3)

4th Latch Output

Table 9: Output to TPC Gated-grid Driver Board:

Bit	Name	Description
Bit 0:11	TPC_1-12	Mask for TPC sectors 1:12
Bit 12:15	Unused	Unused
Bit 16:27	TPC_13-24	Mask for TPC secotors 13:24
Bits 28:31	Unused	Unused