Vertex Algorithm for Tuning
l1_vt201_2010_a.rbt

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Change Log:

Date	Description
December 20, 2009	VT201 tuning algorithm created.

All threshold bits of the Vertex tree from the large and small-tile BBC, the ZDC and the VPD are brought into the Vertex DSM. They are passed on to the TCU. In parallel all four TAC differences are brought into the Vertex DSM. Windows are placed around each TAC difference, and the "inside window" bits get passed through to the TCU and the scaler system. The four MSB of the TAC difference from the BBC small-tiles, the ZDC and the VPD are also in the scaler output. A minimum bias bit, based on an OR of information from all 4 detectors is created. Finally, the atomcules logic is also implemented here.

RBT File: l1_vt201_2010_a.rbt

Users: VT201

Inputs: Ch 0 = BB101
Ch 1 = BB102
Ch 2 = ZD101
Ch 3 = Unused
Ch 4 = VP101
Ch 5:7 = Unused

From Small tile BBC-DSM BB101
(0-12) Small tile TAC-Difference
(13) Unused
(14/15) Small tile ADC East/West sum > th0

From Large tile BBC-DSM BB102
(0-12) Large tile TAC-Difference
(13) Unused
(14/15) Large tile ADC East/West sum > th0

From ZDC DSM ZD101
(0-8) ZDC TAC-Difference
(9) ZDC West gated analog sum > th0
(10) ZDC West analog sum > th1
(11) ZDC West analog sum > th2
(12) ZDC East gated analog sum > th0
(13) ZDC East analog sum > th1
(14) ZDC East analog sum > th2
(15) ZDC East+West attenuated sum > th0

From VPD-DSM VP101
(0-12) VPD TAC-Difference
(13) Unused
(14/15) VPD ADC East/West> th0

LUT: Either 1-to-1 or TAC-difference range conversion

Registers:

R0: BBCsmall-TACdiff-Min (13 bits)
R1: BBCsmall-TACdiff-Max (13)
R2: BBClarge-TACdiff-Min (13)
R3: BBClarge-TACdiff-Max (13)
R4: ZDC-TACdiff-Min (9)
R5: ZDC-TACdiff-Max (9)
R6: VPD-TACdiff-Min (13)
R7: VPD-TACdiff-Max (13)
R8: Minimum-Bias-Select (4)
R9: Atomcules-Central-Select (5)
R10: Atomcules-Waiting-Int-Select (4)
R11: Atomcules-Triggering-Int-Select (4)
R12: Atomcules-Wating-Time (5)
R13: Atomcules-Trigger-Time (5)

Action

1st Latch inputs

2nd Delay the threshold bits from BBC-small, BBC-large, and VPD to the 3rd step along with ZDC th0 bits and ZDC attenuated sum bit.
Delay a second copy of all of these bits to the 4th step.
Combine the ZDC th1 and th2 bits to make windows on the East and West sides separately, i.e.:

ZDC-East-Window = ZDC-E>th1 and not ZDC-E>th2
ZDC-West-Window = ZDC-W>th1 and not ZDC-W>th2

Combine the threshold bits from BBC-small, BBC-large, ZDC and VPD to make the atomcules waiting-stage interaction bit. Use R10 to turn each component on/off, i.e.:

Waiting_int = (R10(0) and (BBC-S-E>th0 or BBC-S-W>th0)) or
(R10(1) and (BBC-L-E>th0 or BBC-L-W>th0)) or
(R10(2) and (ZDC-E>th0 or ZDC-W>th0)) or
(R10(3) and (VPD-E>th0 or VPD-W>th0))

Combine the threshold bits from BBC-small, BBC-large, ZDC and VPD to make the atomcules triggering-stage interaction bit. Use R11 to turn each component on/off, i.e.:

Triggering_int= (R11(0) and (BBC-S-E>th0 or BBC-S-W>th0)) or
(R11(1) and (BBC-L-E>th0 or BBC-L-W>th0)) or
(R11(2) and (ZDC-E>th0 or ZDC-W>th0)) or
(R11(3) and (VPD-E>th0 or VPD-W>th0))

Check each of R12 and R13 to see if they are non-zero. If either is zero then the appropriate stage of the atomcules logic is disabled.

Delay a copy of the BBC-small, VPD and ZDC TAC difference to the 4th step. Compare each of the 4 TAC differences to its minimum and maximum value, as specified in the relevant registers. The logic looks for the TAC difference to be greater than the minimum and less than the maximum;

3rd Combine the results of the TAC difference comparisons to determine if each TAC difference is inside its specified window, e.g.:

ZDC-TAC-diff-in-window = R4 < ZDC TAC difference < R5

Combine the results of the TAC difference comparisons to make the minimum bias bit, using R8 to turn each component on/off, i.e.:

MinB = (R8(0) and BBC-Small-TAC-diff-in-window) or
(R8(1) and BBC-large-TAC-diff-in-window) or
(R8(2) and ZDC-TAC-diff-in-window) or
(R8(3) and VPD-TAC-diff-in-window)

Combine the results of the TAC difference comparisons with the threshold bits to make the atomcules central bit, Use R9 to turn each component on/off, i.e.:

Cent = ((R9(0) and BBC-S-E>th0 and BBC-S-W>th0 and BBC-Tdiff) or not R9(0)) and
((R9(1) and VPD-E>th0 and VPD-W>th0 and VPD-Tdiff) or not R9(1)) and
((R9(2) and ZDC-E>th0 and ZDC-W>th0 and ZDC-Tdiff) or not R9(2)) and
((R9(3) and not ZDC-E+W>th) or not R9(3)) and
((R9(4) and BBC-L-E>th0 and BBC-L-W>th0) or not R9(4))

If there is a central interaction, and R12 is non-zero, then initialize the Waiting-Counter to R12-1. Allow it to count down to zero at a rate of one count per tick of the RHIC clock. Stop counting if a waiting interaction (Waiting_int) occurs while counting is in progress.
If the counter reaches zero without being stopped, and R13 is non-zero, then initialize the Triggering-Counter to R13-1. Allow it to counter down to zero at a rate of one count per tick of the RHIC clock. Stop counting if a triggering interaction (Triggering_int) occurs while this second stage of counting is in progress.
The Atomcules output bit is set while the Triggering-Counter is counter.
NOTE: If R12 is zero then the waiting stage is disabled so the triggering stage

4th Latch Outputs

Output to TCU:

Bit	Name	Description
Bit 0	BBC-TAC	BBC small-tile TAC difference in window
Bit 1	BBC-E	BBC small-tile East ADC sum > threshold
Bit 2	BBC-W	BBC small-tile West ADC sum > threshold
Bit 3	BBC-L-TAC	BBC large-tile TAC difference in window
Bit 4	BBC-L-E	BBC large-tile East ADC sum > threshold
Bit 5	BBC-L-W	BBC large-tile West ADC sum > threshold
Bit 6	ZDC-TAC	ZDC TAC difference in window
Bit 7	ZDC-E	ZDC East gated analog sum > threshold
Bit 8	ZDC-W	ZDC West gated analog sum > threshold
Bit 9	ZDC-UPC	ZDC East analog sum in window AND ZDC West analog sum in window
Bit 10	ZDC-EW	ZDC East+West attenuated sum > threshold
Bit 11	Minimum-Bias	At least one selected TAC difference in window
Bit 12	Atomcules	Central collision followed by a period of no interactions
Bit 13	VPD-TAC	VPD TAC difference in window
Bit 14	VPD-E	VPD East ADC sum > threshold
Bit 15	VPD-W	VPD West ADC sum > threshold

Output to Scalers

Bit	Description
Bit 0	BBC small-tile TAC difference in window
Bits 1:4	4 MSB of BBC small-tile TAC difference
Bit 5	BBC large-tile TAC difference in window
Bit 6	ZDC TAC difference in window
Bits 7:10	4 MSB of ZDC TAC difference
Bit 11	VPD TAC difference in window
Bits 12:15	4 MSB of VPD TAC difference