

Implementation of QT Algorithm for BBC-Small Tiles and VPD qt32b_10_v5_6.mcs

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03/02/2009

Description:

This algorithm forms a 16bit ADC Sum and 12bit TAC Max. Only channels that satisfy a “good hit” requirement are included in the ADC Sum and TAC Max. A “good hit” is defined as one where the ADC value is greater than some threshold and the corresponding TAC value is greater than TAC_MIN and less than TAC_MAX. The channel mask register can be used but note that ADC and TAC channels must each be masked individually.

Inputs:

QT8A: 4 PMT ADC, 4 PMT TAC
QT8B: 4 PMT ADC, 4 PMT TAC
QT8C: 4 PMT ADC, 4 PMT TAC
QT8D: 4 PMT ADC, 4 PMT TAC

Registers (1 Set Per Daughter Card):

Alg. Reg. 0 (Reg 13): ADC_Threshold
Alg. Reg. 1 (Reg 14): TAC_MIN
Alg. Reg. 2 (Reg 15): TAC_MAX
Reg. 11: Channel Mask

LUT:

Timing adjustments/pedestal subtraction for each PMT

Algorithm Latch: 1 or 2

L0 Output to DSM:

(0-15) : ADC Sum
(16-27) : TAC Max
(28-31) : ‘0’