Last DSM Algorithm
2009 Version N – Production PP Running

26th June 2009

Input Bits

NOTE: Only those bits that are used in this algorithm are listed here.

Input Channel	Bit Description	Name
0	TOF,PP2PP and MTD Information	
	Bit 0 – MTD trigger	MTD
	Bits 1:15 - Unused	
1	VTX Information	
	Bit 0 – BBC TAC difference in window	BBC-TAC
	Bit 1 – BBC East ADC sum > threshold	BBCE
	Bit 2 – BBC West ADC sum > threshold	BBCW
	Bits 3:5 – Unused	
	Bit 6 – ZDC TAC difference in window	ZDC-TAC
	Bit 7 – ZDC East ADC sum > threshold	ZDCE
	Bit 8 – ZDC West ADC sum > threshold	ZDCW
	Bit 9 – ZDC East Front ADC > threshold	ZDCE-Front
	Bit 10 – ZDC East Back ADC > threshold	ZDCE-Back
	Bit 11 - ZDC West Front ADC > threshold	ZDCW-Front
	Bit 12 – ZDC West Back ADC > threshold	ZDCW-Back
	Bit 13 – VPD TAC difference in window	VPD-TAC
	Bit 14 – VPD East ADC sum > threshold	VPDE
	Bit 15 – VPD West ADC sum > threshold	VPDW
2	TOF, PP2PP and MTD Information	
	Unused	
3	EMC Information	
	Bits 0:3 – Barrel HT bits	BHT(0:3)
	Bits 4:5 – Endcap HT bits	EHT2 and EHT4
	Bit 6 – Barrel+Endcap jet patch 1	JP1
	Bit 7 – Barrel+Endcap jet patch 2	JP2
	Bit 8 – Barrel-only jet patch 1	BJP1
	Bit 9 – Unused	
	Bit 10 – Endcap-only jet patch 1	EJP1
	Bit 11 – Unused	
	Bit 12 – Barrel+Endcap adjacent jet patch	AJP
	Bits 13:15 – Unused	
4	RAT Board	
	Bit 0 – FMS led	FMS-led
	Bits 1:7 – Unused	
	Bits 8:15 – Detector status [1=Live, 0=Busy]	status(0:7)
5	FMS/FPD Information	
	Bits 0:2 – FMS small-cell cluster threshold bits	FMS-small(0:2)
	Bits 3:5 – FMS small-cell multi-cluster threshold bits	FMS-s-multi(0:2)
	Bit 6 – FMS small-cell HT threshold bit	FMS-small-HT
	Bits 7:9 – FMS large-cell cluster threshold bits	FMS-large(0:2)
	Bits 10:12 – FMS large-cell multi-cluster threshold bits	FMS-l-multi(0:2)

	Bit 13 – FMS large-cell HT threshold bit Bit 14 – FPE trigger Bit 15 - Unused	FMS-large-HT FPE
6	Special Trigger Requests Bits 0:13 - Unused Bit 14 – Zero-bias bit Bit 15 - Unused	Zerobias
7	Unused	

Registers

Register Number	Name	Size (bits)
0	BBCMBLive-PS-lo	12
1	BBCMBLive-PS-hi	12
2	VPDMBLive-PS-lo	12
3	VPDMBLive-PS-hi	12
4	ZDCMB-PS-lo	12
5	ZDCMB-PS-hi	12
6	BBC-Live-Det-Select	8
7	VPD-Live-Det-Select	8
8	Output-Bit1-Select	3
9	Output-Bit2-Select	4
10	JP1-Select	4
11	FMS-Fast-Select	4
12	FMS-led-FPE-Select	2
13	FMS-Slow-Select	3
14	FMS-Fast-Single-PS	8

Output Bits

Bit	Name
Bits 0:15	
0	BIT1
1	BIT2
2	BHT-0
3	BHT-1
4	VPDMB
5	EHT2
6	JP1-selected
7	BBCMBLive-pre
8	VPDMBLive-pre
9	ZDCMB-pre
10	ZDCpol
11	MTD
12	FMSfast
13	FMSslow
14	FMSled-FPE
15	Zerobias
Bits 16:31	Same definitions as bits 0:15

Internal Logic

- BIT1 is a combination (OR) of bits from the BEMC with the BBCMB bit. The bits in register 8 are used to turn each component of BIT1 on or off, i.e.:
  BIT1 = (BHT(3) and reg8(0)) or
  ([BHT(2) and BJP1] and reg8(1)) or
  ([BHT(2) and BBCMB] and reg8(2))
  BBCMB is the BBC minimum bias bit (see below). If the value of register 8 is set to 7 (i.e. "111" in binary notation) then all three components will be included and BIT1 should operate as originally planned.

- BIT2 is a combination (OR) of bits from the EEMC and the combined BEMC+EEMC. The bits in register 9 are used to turn each component of BIT2 on or off, i.e.:
  BIT2 = (JP2 and reg9(0)) or
  (AJP and reg9(1)) or
  (EHT4 and reg9(2)) or
  ([EHT2 and EJP1] and reg9(3))
  If the value of register 9 is set to 15 (i.e. "1111" in binary notation) then all three components will be included and BIT2 should operate as originally planned.

- Bits 2 and 3, BHT-0 and BHT-1, are the first 3 barrel high tower bits [BHT(0:2)] encoded into a 2-bit integer. The 3 HT threshold values that produce these bits are assumed to be sized ordered: i.e. threshold 0 < threshold 1 < threshold 2. The result is that there are only certain combinations of those 3 bits that are physically possible. The logic that encodes the three bits into a 2-bit integer uses this assumption to allow it to zero out unphysical combinations of BHT(0:2)

BHT(0:2)	Meaning	Output integer
0	No HT above any threshold	0
1	At least one HT over (lowest) threshold 0	1
3	At least one HT over (medium) threshold 1	2
7	At least one HT over (high) threshold 2	3
Other combinations	Error – unphysical combination	0

- The VPD minimum bias bit (VPDMB) is a combination of bits from the VPD, i.e.:
  VPDMB = VPD-TAC and VPDE and VPDW

- The EHT2 input bit received on channel 3 is passed through to the output unmodified.

- JP1-selected is a combination (OR) of bits from the BEMC and EEMC. The bits in register 10 are used to turn each component of JP1-selected on or off, i.e.:
  overlap_JP1 = JP1 and not (BJP1 or EJP1)
  JP1-selected = (JP1 and reg10(0)) or
  (BJP1 and reg10(1)) or
  (EJP1 and reg10(2)) or
  (overlap_JP1 and reg10(3))

  NOTES:
  overlap_JP1 represents the JP1 bit from the two jet patches that overlap the BEMC:EEMC boundary.
  IF IT IS WORKING CORRECTLY, the JP1 bit that is received from EM201 on bit 6 of channel 3 is already the OR of BJP1, EJP1 and the JP1 bit from the overlap patches. Commissioning triggers using this bit was found to be complicated because of all the different components. So this new logic, using register 10, was created to make it possible to trigger on just the components instead of the fully combined bit. The components BJP1 and EJP1 are received from EM201 independently on bits 8 and 10 of channel 3. The overlap JP1 bit is NOT received from EM201

independently, so it has to be reconstructed from the bits that are received. This means there only a few values for register 10 that are sensible:

Register 10 Value		JP-selected Behavior
Decimal	Binary	
0	0000	None (turned off)
1	0001	JP1
2	0010	BJP1
4	0100	EJP1
6	0110	BJP1 or EJP1
8	1000	Overlap-JP1

- The BBC minimum bias bit (BBCMB) is a combination of bits from the BBC, i.e.:
  BBCMB = BBC-TAC and BBCE and BBCW
  The BBC-related "Live" bit is calculated using the 8 detector status bits received from the RAT board on channel 4, with the list of requested detectors specified in register 6, i.e.:
  BBCDetLive = ((status(0) and reg6(0)) or not reg6(0)) and
  ((status(1) and reg6(1)) or not reg6(1)) and etc…
  These two bits are then combined to give:
  BBCMBLive = BBCMB and BBCDetLive
  The BBCMBLive bit is then prescaled using the 24-bit value specified in registers 0 and 1. Whenever either of those registers is changed, the prescale counter is initialized to half of the new 24-bit value (i.e. value>>1). Subsequently, the prescale counter is decremented by 1 every time BBCMBLive is true. The output bit, **BBCMBLive-pre,** is set whenever the prescale counter reaches 1. At that point, the counter is also reset to the full starting value specified in registers 0 and 1.

- As explained above, the VPD minimum bias bit (VPDMB) is a combination of VPD bits, i.e.:
  VPDMB = VPD-TAC and VPDE and VPDW
  The VPD-related "Live" bit is calculated using the 8 detector status bits received from the RAT board on channel 4, with the list of requested detectors specified in register 7, i.e.:
  VPDDetLive = ((status(0) and reg7(0)) or not reg7(0)) and
  ((status(1) and reg7(1)) or not reg7(1)) and etc…
  These two bits are then combined to give:
  VPDMBLive = VPDMB and VPDDetLive
  The VPDMBLive bit is then prescaled using the 24-bit value specified in registers 2 and 3. Whenever either of those registers is changed, the prescale counter is initialized to half of the new 24-bit value (i.e. value>>1). Subsequently, the prescale counter is decremented by 1 every time VPDMBLive is true. The output bit, **VPDMBLive-pre,** is set whenever the prescale counter reaches 1. At that point, the counter is also reset to the full starting value specified in registers 2 and 3.

- The ZDC minimum bias bit (ZDCMB) is a combination of bits from the ZDC, i.e.:
  ZDCMB = ZDC-TAC and ZDCE and ZDCW
  The ZDCMB bit is then prescaled using the 24-bit value specified in registers 4 and 5. Whenever either of those registers is changed, the prescale counter is initialized to half of the new 24-bit value (i.e. value>>1). Subsequently, the prescale counter is decremented by 1 every time ZDCMB is true. The output bit, **ZDCMB-pre,** is set whenever the prescale counter reaches 1. At that point, the counter is also reset to the full starting value specified in registers 4 and 5.

- ZDCpol is a combination of bits from the ZDC and BBC, i.e.:
  ZDCpol-E = BBCE and BBCW and ZDCE-Front and ZDCE-Back
  ZDCpol-W = BBCE and BBCW and ZDCW-Front and ZDCW-Back
  ZDCpol = ZDCpol-E or ZDCpol-W

- The MTD input bit received on channel 0 is passed through to the output unmodified.

- FMSfast is a combination (OR) of bits from the FMS single-cluster, multi-cluster and high tower logic. The bits in register 11 are used to turn each component on and off.
  FMSfast = ([FMS-small(1) or FMS-large(1)] and reg11(0)) or
  ([FMS-small-HT or FMS-large-HT] and reg11(1)) or
  ([FMS-s-multi(0) or FMS-l-multi(0) or
  (FMS-small(0) and FMS-large(0))] and reg11(2)) or
  (prescaled([FMS-small(0) or FMS-large(0)] and reg11(3)))
  The prescale logic for the 4th component is implemented in the same way as the prescale logic for the BBC, VPD and ZDC minimum bias bits. An extra-fast FMS bit is made from the OR of the lowest threshold cluster bits for the large and small cells. That bit is turned on or off using the 4th bit of register 11. The result is then prescaled using the 8-bit value specified in register 14. Whenever that register is changed, the prescale counter is initialized to half of the new 8-bit value (i.e. value>>1). Subsequently, the prescale counter is decremented by 1 every time the extra-fast bit is true. The output bit is set whenever the prescale counter reaches 1. At that point, the counter is also reset to the full starting value specified in register 14.

- FMSslow is a combination (OR) of different bits from the FMS single-cluster, multi-cluster and high tower logic. The bits in register 13 are used to turn each component on and off. The combination is vetoed by the FMS LED bit.
  FMSslow = { ([FMS-small(2) or FMS-large(2)] and reg13(0)) or
  ([FMS-small-HT or FMS-large-HT] and reg13(1)) or
  ([FMS-s-multi(2) or FMS-l-multi(2) or
  (FMS-small(2) and FMS-large(2))] and reg13(2)) }
  and not FMSled

- FMSled-FPE is a simple combinations of the led bit received on channel 4 and the FPE bit received on channel 5. The bits in register 12 are used to turn each component on and off.
  FMSled-FPE = (FMSled and reg12(0)) or
  (FPE and reg12(1))

- The zero-bias input bit received on channel 6 is passed through to the output unmodified.