Last DSM Algorithm
2009 Version O – PP2PP Running

30th June 2009

Input Bits

NOTE: Only those bits that are used in this algorithm are listed here.

Input Channel	Bit Description	Name
0	TOF,PP2PP and MTD Information	
	Bit 0 – Unused	
	Bit 1 – PP2PP ET	ET
	Bit 2 – PP2PP ITE	ITE
	Bit 3 – PP2PP ITW	ITW
	Bit 4 – TOF multiplicity > threshold	TOF
	Bits 5:15 - Unused	
1	VTX Information	
	Bit 0 – BBC TAC difference in window	BBC-TAC
	Bit 1 – BBC-small East ADC sum > threshold	BBCE
	Bit 2 – BBC-small West ADC sum > threshold	BBCW
	Bit 3 – Unused	
	Bit 4 – BBC-large Bit 1	BBCL-1
	Bit 5 – BBC-large Bit 2	BBCL-2
	Bit 6 – Unused	
	Bit 7 – ZDC East ADC sum > threshold	ZDCE
	Bit 8 – ZDC West ADC sum > threshold	ZDCW
	Bits 9:12 – Unused	
	Bit 13 – VPD TAC difference in window	VPD-TAC
	Bit 14 – VPD East ADC sum > threshold	VPDE
	Bit 15 – VPD West ADC sum > threshold	VPDW
2	TOF, PP2PP and MTD Information	
	Unused	
3	EMC Information	
	Unused	
4	RAT Board	
	Bit 0 – Unused	
	Bit 1 – Spare (to be defined)	RAT1
	Bits 2:15 – Unused	
5	FMS/FPD Information	
	Bits 0:2 – FMS small-cell cluster threshold bits	FMS-small(0:2)
	Bits 3:6 Unused	
	Bits 7:9 – FMS large-cell cluster threshold bits	FMS-large(0:2)
	Bits 10:15 – Unused	
6	Special Trigger Requests	
	Bits 0:14 - Unused	
	Bit 15 – Random trigger	Random
7	Unused	

Registers

Register Number	Name	Size (bits)
0	ITEW-PS	12

Output Bits

Bit	Name
Bits 0:15	
0	ET
1	ITE
2	ITW
3	TOF
4	BBCE
5	BBCW
6	BBCL-1
7	BBCL-2
8	ZDCE
9	ZDCW
10	RAT1
11	ITEW-pre
12	FMSfast
13	BBC-TAC
14	VPDMB
15	Random
Bits 16:31	Same definitions as bits 0:15

Internal Logic

- The ITEW bit is a combination of pp2pp bits, i.e.:
  ITEW = ITE and ITW
  The ITEW bit is then prescaled using the 12-bit value specified in register 0. Whenever that register is changed, the prescale counter is initialized to half of the new 12-bit value (i.e. value>>1). Subsequently, the prescale counter is decremented by 1 every time ITEW is true. The output bit, **ITEW-pre,** is set whenever the prescale counter reaches 1. At that point, the counter is also reset to the full starting value specified in register 0.

- FMSfast is a combination (OR) of bits from the FMS single-cluster data. The middle threshold (of three) is used because the lowest threshold is set for the multi-cluster triggers.
  FMSfast = FMSsmall(1) or FMSlarge(1)

- The VPD minimum bias bit (VPDMB) is a combination of bits from the VPD, i.e.:
  VPDMB = VPD-TAC and VPDE and VPDW

- All other output bits are just copies of the relevant input bit.