Requirements for QT-based Time-to-Amplitude-Converter (TAC)

Hank Crawford, Jack Engelage, Eleanor Judd, Michael Ng, Chris Perkins
and Gerard Visser

The STAR detector at RHIC uses three sets of detectors in determining the vertex location of an interaction for the level 0 trigger logic. These are the Vertex Position Counters (VPD), the Beam-beam-Counters (BBC) and the Zero-Degree-Calorimeters (ZDC). There are two sets of each detector type, one on the east side of the intersection diamond and one set on the west side. The vertex location is determined by measuring the time difference between when particles from an interaction hit detectors on the east and west sides. All of these detectors use photomultiplier tubes (PMT) to detect photons produced by the energetic particles.

When one of the PMTs detects a photon, a pulse is produced that is sent to an input channel on a QT board. Upon arrival at the QT board, a copy of the pulse is sent to an integrator and another copy is discriminated and compared to a threshold to determine whether a logic pulse should be produced. The logic pulse will be used to start a current source on the proposed TAC that will be stopped by a timing signal from the accelerator, the RHIC Clock (RC, 9.37 MHz). Routing this current source to and input on a QT-8 board where it can be integrated, will yield a charge which is proportional to this time interval. The charge is then digitized. Comparing the digitized values from the east and west sides for each detector will allow a determination of the vertex location for the interaction. This note describes the requirements for the TAC board on which the time interval current is generated.

1. Requirement: Dynamic range

Determine interaction vertices over a range of +/- 3m. to +/-10m.

Justification: The acceptance of the STAR detector is +/- 2m centered on the interaction diamond.

Status: The QT utilizes a dual integrator front end for the ADC. Thus, the integrator can be live during a gate time whose leading edge and width can be anywhere within the 105ns RHIC clock. This fulfills the requirement as it sets an upper limit to the dynamic range of over 30m.

2. Requirement: Resolution

The system must provide an electronic resolution such that the electronics is not the limiting factor

Justification: The acceptance of the inner tracking detectors at STAR is small and has its best performance for interactions within the center of the diamond.

Status: A sigma on the resolution of ~8cm after slewing was achieved by the VPD for events with refmult>6 (Ruan 17-dec-07), the ZDC has routinely returned a resolution sigma of ~31cm (xu 13-jan-05), and the BBC has achieved a resolution sigma 7cm +/-1 (bland 27-jan-04) for high multiplicity events. Thus a position resolution of <4cm for the minimum dynamic range (corresponding to a timing resolution of ~100 ps) is desired .

3. Requirement: Output current per channel

Current output per channel must be < 10 ma. into 50 ohms.

Justification: We want the resolution of our electronics to be better than the resolution of the input detectors (see requirement 2 above).

Status: The QT ADC to be fed by the TAC has a 12 bits range, and a sensitivity of 0.5 pc/count. The limit of QT digitizer noise is well under 1 channel sigma. For a 100ps sensitivity and 0.5 pc/count in the QT ADCs this means 0.5pc/100ps=5ma. At this resolution the 12 bit QT ADC will have a dynamic range in excess of +/- 60m. (previously, to investigate noise sources a +/- 10m range was required.).

4. Requirement: Reproduction of input

The board must provide an output signal for each input logic signal.

Justification: A single discriminator signal is produced for each PMT, and these signals are useful for scaler input as well as TAC and other logic applications.

Status: Our present thinking has the PMT->QT->TAC->QT, with only one output per channel from each QT. We would like to use individual PMT logic signals in the scaler system for monitoring beam and spin operations. An additional copy of the input signals may prove useful in the pre-trigger formulation. This output could be provided on a 34 pin connector for compactness and entails essentially no additional complexity in design. The output signal should be PECL to match the scaler input and 10ns to 100ns wide to accommodate the scaler boards.

5. Requirement: Latency

The output leading edge of the current pulse must be available to feed a QT channel within 30ns of the input leading edge of pmt signal to QT8 .

Justification: Within the timing constraints of the setup this allows us to use a single RC tick for the TAC operation, keeping the hit ADC and the TAC ADC in the same crossing. Maximum dynamic range is 10m or ~35ns, thus RHIC stop to TAC is 35ns from minimum start signal. Maximum current signal to be integrated is hence 35ns. This accounts for 70ns of available 105ns time window (leaving 30ns assuming 5ns for QT to discriminate signal and route to TAC)

6. Requirement: Single stop channel

The board must use a single signal to stop all of the 16 current sources.

Justification: There is no need to use more than a single STOP signal per board.

Status: The source will be RHIC clock (need to determine origin of clock: e.g. P2/J2 backplane? 20-pin TCD cable? 10pin RCF cable?)

7. Requirement: Delay on STOP

There must be a settable delay for the stop signal covering 105ns in increments of <5ns.

Justification: We expect the input channels to be aligned on input to the QT, but the stop signal is from the RC and will need to be delayed to match the input signals to the dynamic range (and resolution?) requirements.

Status: delay setting via VME register if QT daughter card form factor chosen. A front panel switch selectable delay is fine on the front panel of the board if 6u backplane form factor.

8. Requirement: Board Form factor

The TAC board must fit into the VME crate framework.

Justification: VME is the STAR trigger standard crate and power supply system.

Status: need to decide if board will be 6u backplane card or QT daughter card.

9. Requirement: 16 channels per board

Each TAC board must accommodate 16 channels of input.

Justification: All STAR trigger logic is based on 16 channel boards.

Status: the intended input detectors BBC, VPD and ZDC give naturally 16 channels. Individual inputs will have their leading edges aligned by cable length at the input to the QT system, so no individual delays are required on this board.

10. Requirement: Input Form Factor

Input must be differential PECL

Justification: Discriminated signal input from QT is differential PECL (as is RCF clock signal)

Status: QT discriminator signal is output on outer rows of P2/J2 VME DIN connector. Physical connection between QT VME DIN and TAC board will depend on requirement 10 (e.g. 6U back of crate -> P2 overlay, QT daughter card -> 34pin IDC, etc.)

11. Requirement: output form factor

The output current must be a negative polarity (<4V max) available on positronix connector (i.e 2 positronix assemblies for total of the 16 channels).

Justification: This output will feed 2 QT-8 daughter cards

12. Requirement: Monitor output

The board must provide a copy of the stop signal and at least one input channel for monitor purposes.

Justification: ease of testing.

Status: Should be a 2pin BERG output for each mounted such that access by differential scope probe is possible.