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Requirements for Scaler Board II

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The current scaler boards, referred to as scaler-I, allow for 24 input bits acting as address bits in a histogramming memory, but they take more than 1 minute to read a typical randomly populated board. With multiple boards in use the total readout time for the scaler system often exceeds 2 minutes. Since STAR data runs are typically 20 minutes long this amounts to imposing a 10% deadtime. The new boards are being designed to minimize this deadtime by implementing a different readout scheme which is enabled by the great increases in local CPU memory available since scaler-I was designed.

Our current thinking involves making multiple linux boxes each having 1 or more scaler boards on its PCI bus. Each board would control two memory blocks so that one block would be being filled while the other was being read out. Each memory block would be at least 2^{24}X9B = 151 MB (million bytes). Data would be stored in the local CPU memory and then shipped via Ethernet to the database machines to keep the scalers alive essentially 100% of the time. Synchronization with the STAR system would be accomplished through a RUN/STOP level input to each board.

1. Requirement: Input bits: Each board must accept 30 input bits that act as address bits for a histogramming memory.
Justification: The current 24 bit system has provided adequate polarimetry, typically using 7 bits for bunch ID, 16 bits for detector input, and 1 bit for checking integrity of each board: however, we want to increase the bit count to allow better correlation measurements.
Status: 128 MB (3B addr + 8B deep) of memory is small by today's standards and we will use up to 30 input bits requiring therefore 8 GB per memory.

2. Requirement: Input bit delays: Each input channel must have both fine (clock*8) and coarse (Clock(<20 MHz)) delays to allow alignment of input bit pulses to a common clock cycle.
Justification: The DSMs and QTs produce levels on their outputs that are fed to the RAT board and then into scaler boards. These levels do not change if the conditions driving the output do not change. The timing adjustments are to catch the leading edge of a changing level.

3. Requirement: Input bit alignment: Each channel must have a register selectable one-shot option to allow setting a "TRUE" level on the leading edge of the input pulse, resetting it to "FALSE" 2 ns after it has been latched for input.
Justification: Some of the scaler input comes from signals that have varying timing within a crossing and varying widths depending on input signal.

4. Requirement: Signal standard: Boards must accept PECL input signals.

Justification: DSM and QT outputs are PECL levels.

5. Requirement: clock: The board must accept a clock signal that drives all internal timing.
Justification: STAR runs as a synchronous system.
Status: the experiment clock originates in an RCC board.

6. Requirement: Histogram address Latch : The board must take the address of the histogram cell from the input levels latched at the rising edge of each input clock pulse.
Justification: The board is used to record hits and logic combinations for each crossing at STAR.

7. Requirement: Memory: The histogramming memory must be at 30 bits wide and 40 bits deep.
Justification: The 30 input bits allow detector-beam correlations. The 40 bits deep allows operating for more than 24 hours without restarting.
Status: the old boards used 24bit address with 40 bit depth or 8B per channel. Using 30 bits and 40 bits is almost 9B per channel.

8. Requirement: Ping-Pong: Boards must be able to acquire data without interruption while histogramming memory is being read.
Justification: We currently record data in every crossing and we need to continue this practice. The ping-pong concept is currently used at the board level, but will be implemented on each board at the memory level to allow simultaneous reading ad acquisition.

9. Requirement: Start/Stop: The histogramming memory must be able to start and stop within a single clock cycle under control of a register-selectable input signal.
Justification: All memory cells must sample the same live time.

10: Requirement: Readout: The histogramming memory must be able to be read without impacting STAR's data taking ability.
Justification: Readout currently shuts STAR down because we want the scalers to be synchronous with the experiment and to record data whenever STAR is taking data.

11. Requirement: Startup: The board must be configured to start data taking in less than 10 sec.
Justification: We want to minimize the deadtime attributable to this system and it currently takes about 10sec for the system to start because of other configuration issues.

12. Requirement: Data storage: Scaler data must be made available to a database within 10 minutes of stopping a board.
Justification: Fast offline analysis will use this information to check data quality.

13. Requirement: Form Factor: TBD