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STAR TCDs (2007 TPC version) User Manual

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The Front Panel:

There are 11 LEMO connectors on the front panel All signals are TTL! (logic 1 = +4V) Inputs are terminated with 50 ohms Outputs are capable of driving 50 ohms The connectors (listed in order from top to bottom:

DAQLIVE input
BUSY output
PIN input
MISC IN input
TRIG input
OUT2 output
OUT1 output
OUT4 output
OUT3 output
PUL OUT output NEW Test Fixture **Pad Plane Pulser output**
GRID OUT output

There are 11 LEDs on the front panel

A yellow Led at the top indicates the selection of the local oscillator Below the special trigger request output pins is a yellow LED to indicate a pending 'special request.' Below each of the 6 LEMO outputs there is a green LED to indicate the state of the respective output signal. Above the FPGA configuration port is a red LED to indicate the FPGA is NOT configured. At the bottom of the panel is a red LED to indicate a blown fuse.

There is only one jumper option on the front panel: at the very top a jumper can be used to select the local oscillator; this option is in parallel with CSR bit 4;
The 3 'special trigger request' bits (PECL) are located just below the local oscillator jumper and are cabled to the special request DSM.

Each TCD must be customized to suit the requirements of its subsystem by loading an FPGA configuration file. This configuration can be changed in situ via a front-panel connection to a PC. All configuration files are prepared by Fred Bieser and can be downloaded by Fred or by Dan Padrazo.

The 11 signals listed above have 'nominal' functionality definitions as instantiated in the modules for TPC, FTPC, etc and they are:

DAQLIVE = input from DAQ indicating DAQ is busy (receiving data); this is ORd with local busy to produce a busy signal fed back to the TCU and reflected on the BUSY output LEMO. Neither the DAQ busy nor the internal busy actually prevent triggers from being issued by the TCD unless this inhibition is performed by the TCU or external software in the case of stand-alone operation.

BUSY = output of busy OR (see above)

PIN = input from Laser System to indicate actual Laser Flash

MISC = input from Laser System to indicate a Laser Flash is imminent (10 to 200 microseconds??); this can be used to cause a 'special trigger request' pattern to be sent to the special trigger DSM as an aid in interleaving laser events with physics events with minimal deadtime.

TRIG = input to cause a trigger to be issued (type defined in command register, token numbers auto-incrementing) IF such action is enabled (bit 6 in CSR = 1)

OUT 2 = output (1 RHIC period) for any Level 0 trigger issued from *this* TCD

OUT 1 = output of phase-delayed RHIC strobe (real or local)

OUT 4 = output (1 RHIC period) for any Level 0 trigger of type 4 (physics) issued from *this* TCD

OUT 3 = output (1 RHIC period) for any abort issued from this TCD

PUL OUT = output (1 RHIC period) for any Level 0 trigger of type 10 (padplane pulser) issued from this TCD; used to fire programmable pulser.

This output was modified for Test Fixture (see CSR assignment)

GRID OUT = output (of programmable width) to operate the gated grid drivers; active for all triggers of types 4,5,6,7,8,9, & 10

Deviations from the above list include:

BSMD, SVT: OUT 3 = output (1 RHIC period) for any Level 0 trigger of type 4,5,6,7,8,9,10,11,or 12 issued from this TCD; OUT 2 = undefined; OUT 4 undefined

The VME base address for each TCD is set via jumpers and is, for convenience, assigned according to their physical location in the crate. Detector ID bits (and busy bits) are also

set via jumpers:

VME slot	Base Address	Subsystem	detector ID
6	0x10 000 000	ESMD	9
7	0x11 000 000	BBC	15
8	0x12 000 000	ETOW	8

9	0x13 000 000	SSD	5
10	0x14 000 000	FPD	7
11	0x15 000 000	TOF	4
12	0x16 000 000	SVT	1
13	0x17 000 000	reserved	-
14	0x18 000 000	MWC	-
15	0x19 000 000	BSMD	2
16	0x1A 000 000	CTB	14
17	0x1B 000 000	BTOW	6
18	0x1C 000 000	FTPC	3
19	0x1D 000 000	PMD	10
20	0x1E 000 000	TPC	0
21	0x1F 000 000	reserved	-

The jumper locations are labeled VME A24 thru 31; a jumper present = 1

Two fields of 16 jumper locations are also located near the P3 connector and are labeled "Detector Select" and "Detector BUSY." Each TCD should be configured with one jumper to determine the correct subsystem as listed in the detector ID bit list above and (in most cases) which busy bit to use.

Several control and status registers are available via D16 VME access at the module base address plus the indicated offset:

Offset Register Name

0x00 CSR
0x02 Command
0x04 Token
0x06 Phase Delay
0x08 Special Request
0x0A Grid Gate Width

0x0C DAC

0x0E Last Action
0x10 SVT Delay #1

0x12 SVT Delay #2

0x14 Internal Busy Time

0x16 Abort Busy Time

0x18 -

0x1A -

0x1C -

0x1E Detector Bit & Version #

The bits within the CSR are
defined as follows:

15 Local Oscillator Selected (read only)
14 Busy OR: 1 = busy; logical OR of internally generated 'local' busy & inverted DAQLIVE (read only)
13 DAQ Busy: 1 = busy (inverse of front panel DAQ LIVE) (read only)
12 Internal Busy: 1 = busy; (digital timer unique to each subsystem) (read only)
11 **NEW** **RDO Board(s) BUSY** 1 = busy, **signal 'ORed' from all sectors** (read only)

The Ten low order bits are all Read/Write
10 -
9 **NEW** **Mask RDO Board(s) BUSY(set to 1 will ignore busy from RDO Board(s))**
8 Bypass DAQ Busy (set to 1 will assert DAQLIVE regardless of front panel input
7 Force trigger: will issue trigger when CSR accessed with VME Write with this bit set to 1; does not stick, IE must write a 1 each time to trigger
6 Enable Front Panel Trigger: allows triggers to be initiated via front panel TRIG IN signal (trig type and token # from registers)
5 Enable Pretrig: enables Laser pretrig signal (front panel MISC IN) to issue special trigger request to special trigger DSM
4 Select Local Oscillator: ignore ALL P3 signals and use internal oscillator
3 **NEW** **Pulser choice** Set to 1 to choose Pad Plane Pulser for testing in Lab. (delay 128 clock cycles, then high for 128 cycles)
2
1

Command Register: 8 bits composed of 2 nibbles: bits 0,1,2,3 = trigger command and bits 4,5,6,,7 = DAQ command.

Token Register: 16 bits (of which only the lower 12 are used): token number used for next locally initiated trigger.

Phase Delay Register: 8 bits (of which only the lower 7 are used): phase shift in nanoseconds of incoming RHIC strobe from TCU (or internal oscillator if selected) to outputs to Readout System. Caution: do not set greater than 100ns (0x64)

Special Request Register: 8 bits (of which only the lower 3 are used)

setting any of these

bits to 1 will present the bit(s) to the special trigger DSM as a special trigger request. **All** bits will be automatically cleared when *any* Level 0 trigger of command type 8,9,10, or 11 is initiated .

Grid Gate Width: 16 bits: time gating grid is commanded 'open' counted in RHIC ticks from 0 to 32767 or 0x7FFF (approx 3400 microseconds.) **IF** bit 15 is set (values greater than 0x7FFF) then the grid is commanded "open" continuously.

DAC Register: 16 bits intended for use with a Digital to Analog Converter for providing a discriminator voltage to the MWPC front-ends. Not currently implemented. Can be used as a general purpose scratch register.

Last Action Register: 16 bits (read only) reflecting the last trigger command (bits 15,14,13,12) and associated token # (bits 11..0) that *this* module captured from the TCU via the P3 backplane (IE *this* detector's bit was set.)

SVT Delay#1 Register: 16 bit counter (each count = 1 RHIC tick) sets delay from receipt of command of trigger type 4 (physics) until TCD actually sends this command to the SVT readout boxes. Also used by BSMD

SVT Delay#2 Register: 16 bit counter (each count = 1 RHIC tick) sets delay from receipt of command of trigger type 8 (internal pulser) until TCD actually sends this command to the SVT readout boxes. Also used by BSMD

Internal Busy Register: 16 bit counter (each count = 1 RHIC tick) sets time delay from receipt of command until internal Busy expires. (Default = 0)

Abort Busy Register: 16 bit counter (each count = 1 RHIC tick) sets time delay from receipt of abort command until Abort expires. (Default = 0) This is now included in busyor

Detector Bit/Version #: 16 bit read only register that indicates the detector ID of the FPGA code, (IE the detector for which this firmware was prepared, NOT the jumper settings of the module!!) (bits 15,14,13,12) and the revision number of the FPGA firmware (bits 11..0)

The outer rows (A & C) of VME P2 are used to bring out differential (PECL) signals. The first 8 pairs carry signals used by the 'slow' detectors after being fanned out with one or more cable driver cards:

Pin# signal
1 RHIC clock (20 or 40% duty cycle)
2 data bit 0
3 data bit 1
4 data bit 2
5 data bit 3
6 5xRHIC clock
7 custom clk1 (eg. SCA sample clk for the TPC)
8 custom clk2 (eg. Calib. strobe for the MWC)
the next two pairs are open-collector signals coming back from the Front-end to the TCD:
9 busy NEW **Buffered Busy "OR" from all RDO Boards (true low)**
10 status

The above 10 signals are described in more detail in the STAR Trigger-Front-End Interface Document page 19.
the next 20 pairs are intended for use by the 'fast' detectors:

11 Trig command bit 0

12 Trig command bit 1
13 Trig command bit 2
14 Trig command bit 3

15 DAQ command bit 0
16 DAQ command bit 1
17 DAQ command bit 2
18 DAQ command bit 3
19 Token bit 0
20 Token bit 1
21 Token bit 2
22 Token bit 3
23 Token bit 4
24 Token bit 5
25 Token bit 6
26 Token bit 7
27 Token bit 8
28 Token bit 9
29 Token bit 10
30 Token bit 11
The last two pairs are PECL signals coming back from the FEE:

31 busy 1 32
busy 2

Note that the + half of each differential signal is routed to the A side of the 3-row P2 connector while the negative half goes to the C side. A 10-pair 'twist-n-flat' cable with DIN IDC connectors on both ends will properly bring the first ten signals to the cable driver boards in their dedicated crate (located below the TCD crate.) When making a cable that has a DIN IDC connector on one end and a 3M connector on the opposite end (for using the parallel outputs for 'fast' detectors) the +signal ends up on pin 2 of the 3M connector while the negative signal is on pin 1!! This is an unfortunate result of the way the DIN cable connector is designed. One can either wire the destination hardware appropriately *or* cause a pair reversal by inserting a second section of ribbon cable and a male-male inline connector.

Appendix

Laser triggers: laser triggers are tricky because the laser is 'free running' at about 10Hz (In principle it is phase-locked to RHIC via the delayed RHIC strobe output from the front panel of

the sub-system specific TCD.) while the actual trigger command to the Readout system should be synchronized with the actual Laser flash. To accomplish this, the TCD does not automatically send laser triggers (type 9) immediately upon receipt but, rather, catches the 20 bits of TRIG command + DAQ command + Token and waits for a signal on the front panel "PIN" connector. While waiting, local busy is asserted. Beginning with version 6 of the firmware for TPCm and TPCf, this wait can be up to 1 second (after which the trigger command will be sent to the Readout system anyway to prevent hang-ups.) To avoid large deadtimes (average of 50ms) while interspersing Laser triggers with Physics triggers, a 'pretrigger' signal can be used: set bit 5 of the CSR; upon receipt of a pretrigger signal from the Laser, the TCD will assert "special trigger request" bit pattern 010. The TCU should turn this into a command 9 trigger within a few RHIC ticks and then the TCD will only be waiting a few microseconds until it gets the PIN signal from the Laser flash.

Local Oscillator: In the absence of a *running* TCU, there is **NO** RHIC clock and furthermore, all detector bits and all command bits on the P3 backplane are driven high! To operate a TCD in "local oscillator" mode (IE without the TCU) an onboard oscillator (freq. = 9.4348 MHz) can be selected by setting bit 4 of the CSR to 1. This selection will also disable all responses by the TCD to ANY TCU signals on the P3 backplane. When the local oscillator is selected, a yellow LED near the top of the front panel will be illuminated.

Internal Busy: Each subsystem has its own specific requirements for the generation of local busy; in general local busy is used to prevent the TCU from issuing more triggers during the time the readout system is responding to the initial trigger BUT the DAQ receiver has not yet asserted its busy. It is desirable to keep this fixed (minimum) busy time as small as possible but it must be long enough to cover the worst case latency in receiving the DAQ busy signal. Troubles can arise, for example, if the DAQ busy doesn't arrive because the readout system has not started data transmission because it, in turn, is waiting for a Level2 accept that is late (or missing.)

Local Operations: Triggers can be initiated by writing a 1 to bit 7 of the CSR or via a front panel TRIG signal (if enabled.) The TRIG and DAQ Command bits and the token number then come from the command and token registers. While these registers can be loaded with any value, the token register will increment by one *after* each locally initiated trigger. If it is desired to send two consecutive commands with the *same* token number (such as command 4= physics followed by command 15=L2accept) the token register must be rewritten before the second trigger is initiated. These registers are neither affected nor used by 'normal' TCU operations. Note: it is possible to initiate 'local' operations while running on the TCU RHIC clock (local oscillator *not* selected) but this can lead to very confused trigger/DAQ systems as Readout Systems produce data streams that are 'unexpected.' In most cases it will be desirable to set the "bypass DAQ busy" CSR bit while operating in stand-alone mode since the default condition (no "DAQ LIVE" signal connected) means DAQ busy. While the TCD does not actually inhibit any actions while a busy signal is present, the front panel BUSY LED and the CSR bits will still reflect the conditions of the busy signals.