STAR Trigger DSM Register List

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This table lists all the registers in the all the algorithms that are loaded into the STAR Trigger DSM boards. These registers control the operation of the algorithms: setting thresholds on ADC values, putting windows on TAC values and selecting which bits get used to make the trigger decision.

Object	Index	Register	Name	Default value	Bit mask	Description
1			L1			
	19	0	VP101	0xa	0x7ff	VPDE ADC th0
		1		0xa	0x7ff	VPDW ADC th0
		2		0xf	0x7ff	VPDE ADC th1
		3		0xf	0x7ff	VPDW ADC th1
	21	0	CB201	0x7	0x7	Topology Selection Bit 0: veto “out-of-time” hits Bit 1: veto “overflows” Bit 2: use UPC algorithm for topology decision
		1		0x0	0x1ff	VPD DeltaT Min0
		2		0x2	0x1ff	VPD DeltaT Max0
		3		0x0	0x1ff	VPD-DeltaT Min1
		4		0x2	0x1ff	VPD-DeltaT Max1
	23	0	LD301	0x1	0xff	Prescale for VPD bit
		1		0x1	0xff	Prescale for BBC bit
		2		0x1	0xff	Prescale for ZDCE bit
	25	0	VT201	0x0a0	0x1ff	BBC DeltaT Min0
		1		0x160	0x1ff	BBC DeltaT Max0
		2		0x0a0	0x1ff	BBC-DeltaT Min1
		3		0x160	0x1ff	BBC-DeltaT Max1
		4		0x0a0	0x1ff	ZDC-DeltaT Min0
		5		0x160	0x1ff	ZDC-DeltaT Max0
		6		0x0a0	0x1ff	ZDC-DeltaT Min1
		7		0x160	0x1ff	ZDC-DeltaT Max1
		8		0x5	0x7	BBC Small Tile DeltaT Scalar Bit
		9		0x6	0x7	BBC Large Tile DeltaT Scalar Bit
		10		0x5	0x7	ZDC DeltaT Scalar Bit
	26	0	EM201	0x3	0x7	Threshold Select J/Ψ (0,1,2,3,4)
	27	0	BX201	0x0	0xffff	BXing start value: 16 LSB
		1		0x0	0xffff	BXing start value: 16 next bits
		2		0x1	0xffff	Rev Tick synch enable
	28	0	BX202	0x0	0xffff	BXing start: 16 MSB
	29	0	ST201	0x6cd8	0xffff	Zero-bias prescale: 16 LSB
		1		0x1	0xffff	Zero-bias prescale: 16 MSB
		2		0x0	0xfff	Random rate: 12 LSB

		3		0x0	0xfff	Random rate: 12 MSB
	30	0	FP201	0x0	0x3fff	FPD East ADC sum low threshold
		1		0x0	0x3fff	FPD East ADC sum med threshold
		2		0x0	0x3fff	FPD East ADC sum high threshold
		3		0x0	0x3fff	FPD++ S3, S4 threshold 0
		4		0x0	0x7fff	FPD++ S13, S24 threshold 0
		5		0x0	0x3fff	FPD++ S1, S2 threshold 0
		6		0x0	0x3fff	FPD++ S3, S4 threshold 1
		7		0x0	0x7fff	FPD++ S13, S24 threshold 1
		8		0x0	0xffff	FPD++ S1234 threshold 0
		9		0x0	0x7fff	FPD East Sum-NE-SE threshold 0
2			BC1			
remove	33	0	BE101	0	0xfff	BEMC-jet-patch-th0
remove		1		1	0xfff	BEMC-jet-patch-th1
remove		2		2	0xfff	BEMC-jet-patch-th2
remove		3		2	0x3	BEMC-TP-select (1,2,3)
remove		4		2	0x3	BEMC HT.TP-select (1,2,3)
remove	16		BE102			same as 33
remove	17		BE103			same as 33
remove	18		BW101			same as 33
remove	19		BW102			same as 33
remove	20		BW103			same as 33
remove	21	0	EE101	0	0x7ff	EEMC-jet-patch-th0
remove		1		1	0x7ff	EEMC-jet-patch-th1
remove		2		2	0x7ff	EEMC-jet-patch-th2
remove		3		2	0x3	EEMC-TP-select (1,2,3)
remove		4		2	0x3	EEMC-HT.TP-select (1,2,3)
remove	22		EE102			same as 21
	23	0	EE001	0x04	0x3f	EEMC-high-tower-th0
		1		0x09	0x3f	EEMC-high-tower-th1
		2		0x0e	0x3f	EEMC-high-tower-th2
		3		0x01	0x3f	EEMC-high-tower-th3
		4		0x01	0x3f	EEMC-high-tower-th4
		5		0x3ff	0x3ff	EEMC-EE001-th4-bitmask
	24	0:4	EE002			same as 23
		5				EEMC-EE002-th4-bitmask
	25	0:4	EE003			same as 23
		5				EEMC-EE003-th4-bitmask
	26	0:4	EE004			same as 23
		5				EEMC-EE004-th4-bitmask
	27	0:4	EE005			same as 23
		5				EEMC-EE005-th4-bitmask
	28	0:4	EE006			same as 23
		5				EEMC-EE006-th4-bitmask
	29	0:4	EE007			same as 23
		5				EEMC-EE007-th4-bitmask
	30	0:4	EE008			same as 23
		5				EEMC-EE008-th4-bitmask
	31	0:4	EE009			same as 23
		5				EEMC-EE009-th4-bitmask

3			MIX			
	16	0	MD001	0x0	0xff	MTD TAC min
		1		0xff	0xff	MTD TAC max
	18		MD002			Same as 16
	21	0	VP001	0x4	0xff	VPD ADC threshold
		1		0x0	0xff	VPD TAC Min
		2		0xff	0xff	VPD TAC Max
		3		0x0	0xf	VPD ADC threshold deadtime in RS
	23		VP002			same as 21
	25		VP003			same as 21
	27		VP004			same as 21
4			CTB			
	16	0	CB001	0x0	0xf	CTB deadtime in RS's
		1		0x000	0xfff	Min ADC sum for topology alg.
		2		0xfff	0xfff	Max ADC sum for topology alg.
		3		0x0	0xf	Min. slat sun for topology alg.
		4		0xf	0xf	Max. slat sum for topology alg.
	17		CB002			same as 16
	18		CB003			same as 16
	19		CB004			same as 16
5			BCW			
	16	0	BW001	0	0x3f	BEMC-West high-tower-th0
		1		1	0x3f	BEMC-West high-tower-th1
		2		2	0x3f	BEMC-West high-tower-th2
		3		1	0x3f	BEMC-West high-tower-th3
		4		1	0x3f	BEMC-West high-tower-th4
		5		0x3ff	0x3ff	BEMC-BW001-th4-bitmask
	17	0:4	BW002			same as 16
		5				BEMC-BW002-th4-bitmask
	18	0:4	BW003			same as 16
		5				BEMC-BW003-th4-bitmask
	19	0:4	BW004			same as 16
		5				BEMC-BW004-th4-bitmask
	20	0:4	BW005			same as 16
		5				BEMC-BW005-th4-bitmask
	21	0:4	BW006			same as 16
		5				BEMC-BW006-th4-bitmask
	22	0:4	BW007			same as 16
		5				BEMC-BW007-th4-bitmask
	23	0:4	BW008			same as 16
		5				BEMC-BW008-th4-bitmask
	24	0:4	BW009			same as 16
		5				BEMC-BW009-th4-bitmask
	25	0:4	BW010			same as 16
		5				BEMC-BW010-th4-bitmask
	26	0:4	BW011			same as 16
		5				BEMC-BW011-th4-bitmask
	27	0:4	BW012			same as 16
		5				BEMC-BW012-th4-bitmask
	28	0:4	BW013			same as 16
		5				BEMC-BW013-th4-bitmask

	29	0:4	BW014			same as 16
		5				BEMC-BW014-th4-bitmask
	30	0:4	BW015			same as 16
		5				BEMC-BW015-th4-bitmask
6			BCE			
	16	0	BE001	0	0x3f	BEMC-East high-tower-th0
		1		1	0x3f	BEMC-East high-tower-th1
		2		2	0x3f	BEMC-East high-tower-th2
		3		1	0x3f	BEMC-East high-tower-th3
		4		1	0x3f	BEMC-East high-tower-th4
		5		0x3ff	0x3ff	BEMC-BE001-th4-bitmask
	17	0:4	BE002			same as 16
		5				BEMC-BE002-th4-bitmask
	18	0:4	BE003			same as 16
		5				BEMC-BE003-th4-bitmask
	19	0:4	BE004			same as 16
		5				BEMC-BE004-th4-bitmask
	20	0:4	BE005			same as 16
		5				BEMC-BE005-th4-bitmask
	21	0:4	BE006			same as 16
		5				BEMC-BE006-th4-bitmask
	22	0:4	BE007			same as 16
		5				BEMC-BE007-th4-bitmask
	23	0:4	BE008			same as 16
		5				BEMC-BE008-th4-bitmask
	24	0:4	BE009			same as 16
		5				BEMC-BE009-th4-bitmask
	25	0:4	BE010			same as 16
		5				BEMC-BE010-th4-bitmask
	26	0:4	BE011			same as 16
		5				BEMC-BE011-th4-bitmask
	27	0:4	BE012			same as 16
		5				BEMC-BE012-th4-bitmask
	28	0:4	BE013			same as 16
		5				BEMC-BE013-th4-bitmask
	29	0:4	BE014			same as 16
		5				BEMC-BE014-th4-bitmask
	30	0:4	BE015			same as 16
		5				BEMC-BE015-th4-bitmask
7			EEC			This crate no longer exists
8			BBC			
	16	0	BB001	0x4	0xff	BBC small-tile ADC threshold
		1		0x0	0xff	BBC small-tile TAC Min
		2		0xff	0xff	BBC small-tile TAC Max
		3		0x0	0xf	BBC small-tile thr. deadtime in RS's
	18		BB002			same as 16
	20		BB003			same as 16
	22		BB004			same as 16
	24	0	BB005	0x4	0xff	BBC large-tile ADC threshold
		1		0x0	0xff	BBC large-tile TAC Min

		2		0xff	0xff	BBC large-tile TAC Max
		3		0x0	0xf	BBC large-tile thr. deadtime in RS's
	25		BB006			same as 24
	26	0	BB101	0xa	0x7ff	BBCE small-tile ADC th0
		1		0xa	0x7ff	BBCW small-tile ADC th0
		2		0xf	0x7ff	BBCE small-tile ADC th1
		3		0xf	0x7ff	BBCW small-tile ADC th1
	27	0	BB102	0xa	0x7ff	BBCE large-tile ADC th0
		1		0xa	0x7ff	BBCW large-tile ADC th0
		2		0xf	0x7ff	BBCE large-tile ADC th1
		3		0xf	0x7ff	BBCW large-tile ADC th1
	28	0	ZD001	0x5	0xff	ZDCE-ADC-th0
		1		0x5	0xff	ZDCW-ADC-th0
		2		0xf	0xff	ZDCE-ADC-th1
		3		0xf	0xff	ZDCW-ADC-th1
		4		0x0	0xff	ZDCE-TAC-min
		5		0x0	0xff	ZDCW-TAC-min
		6		0xa	0xf	ZDC-th0-deadtime in RS's
		7		0xa	0xf	ZDC-th1-deadtime in RS's
		8		0xa	0xf	ZDC-timewin-deadtime in RS's
		9		0x50	0xff	ZDC-sum-att-th
		10		0x0a	0xf	ZDC-sum-att-deadtime in RS's
		11		0xff	0xff	ZDCE-TAC-max
		12		0xff	0xff	ZDCW-TAC-max
9			FPE			
	23	0	FE101	0xff	0xff	FPE Module bitmask 1 (8 bits)
10			FMS			
	23	0	FW101	0xff	0xff	FPD++ Module bitmask 1 (8 bits)
	28	0	FW102	0xf	0xf	FPD++ Module bitmask 2 (4 bits)

Change Log:

11th January 2005:

Object 1, Index 30, FP201:

Changed "FPD ADC sum low threshold" to "FPD East ADC sum low threshold"
Same for "med" and "high" thresholds.
Changed "Threshold select" to "High-Tower Threshold select". This register is no longer used by the Sum algorithms.
Added registers 5, 6 and 7 "FPD West ADC sum low threshold", "med" and "high".

Object 5, Index 16, BW001:

Changed register names from "BEMC-high-tower-thX" to "BEMC-West high-tower-thX" to distinguish East from West.

Object 6, Index 16, BE001:

Changed register names from "BEMC-high-tower-thX" to "BEMC-East high-tower-thX" to distinguish East from West.

28th October 2004:

FIRST VERSION FOR 2005 RUNNING PERIOD
Added a comment at the beginning to say what these registers are.

Object 1, Index 25, VT201:

Added registers 8, 9 and 10 for "DeltaT Scalar Bit" selection. NOTE: These registers exist but are not actually used yet by the algorithm

Object 8, Index 24, BB005

This BBC large-tile DSM is now using the small-tile algorithms. The original 2 registers were replaced with the 4 registers used by the small-tile algorithms, but the names were changed to indicate this was a large-tile DSM, e.g. “BBC small-tile ADC threshold” became “BBC large-tile ADC threshold:, etc….

Object 8, Index 25, BB006

This new DSM is the second BBC large-tile DSM. It has the same algorithm and registers as Object 8, Index 24, BB005 (see above).

Object 9, Indices 16:22 (FE001:FE007) and 24:27 (FE008:FE011)

Three registers were added to all these DSMs for the FPD high-tower algorithms: “FPD East high-tower-th0”, “th1” and “th2”.

Object 10, Indices 16:22 (FE001:FE007) and 24:27 (FE008:FE011)

Three registers were added to all these DSMs for the FPD high-tower algorithms: “FPD West high-tower-th0”, “th1” and “th2”.

17th March 2006

FIRST VERSION FOR 2006 RUNNING PERIOD

Object 1, Index 23, LD301

Changed the meaning of registers 0-3 and removed register 4 for the 2006 algorithm.

Object 1, Index 26, EM201

Changed the meaning of registers 3 and 4 from jet-patch control to energy-sum control.

Object 1, Index 30, FP201

Added registers 8 and 9 and redefined the meaning of registers 3 to 9 for the new FPD++.

Object 2, Indices 33 and 16:22, BE/BW/EE10X

Added register 3 (TP-select) and register 4 (HT.TP-select)

Object 2, Indices 23:31 (EE001:EE009)

Added registers 3, 4 and 5 for the 3 TP thresholds

Object 5, Indices 16:30 (BW001:BW015)

Added registers 3, 4 and 5 for the 3 TP thresholds

Object 6, Indices 16:30 (BE001:BE015)

Added registers 3, 4 and 5 for the 3 TP thresholds

Object 8, Index 28 (MD001)

Added register 0 for the MTD ADC threshold

Object 9, Indices 16:27 (FE001:FE011)

All registers were removed. These registers were used temporarily while the PFD group tested the high tower algorithms which are no longer in use.

Object 10, Indices 16:27 (FW001:FW011)

All high tower registers were removed (see above)

Object 10, Indices 23 and 28 (FW101 and FW102)

Added register 0 for the module bitmask

21st March 2006

Object 9, Indices 23 and 28 (FE101 and FE102)

Added register 0 for the module bitmask

26th February 2007

FIRST VERSION FOR 2007 RUNNING PERIOD

Object 1, Index 18 (VP101, used to be MW102)

Added this DSM since it is now running the BB101 algorithm for VPD

Object 1, Index 21 (CB201)

Added registers 1:4 for the VPD TAC difference windows

Object 1, Index 23 (LD301)

Removed registers 2 and 3 and renamed registers 0 and 1 to this year’s values

Object 3

Renamed from MWC to MIX

Object 3, Indices 23 and 25 (VP001, VP002)

Added registers 0:3 for these DSMS which are running the BB001 algorithm for VPD

Object 8, Index 28 (MD001)

Removed this register since MTD has been removed from the BBC crate

8th March 2007

Object 3, Indices 16 and 18 (MD001, MD002)

Added these new DSMS with 1 register each for the MTD

Object 3, Indices 21 and 27 (VP001, VP004)

Added these new DSMS to complete the VPD layer 0

17th March 2007

Object 1, Index 23 (LD301)

Added registers 2:5 for the UPC, detector-live and ZDCxLive prescale logic.

3rd April 2007

Object 1, Index 19 (VP101)

Changed the Index from 18 to 19 because VP101 is using the old MW101 at address 0x13 instead of the old MW102 at address 0x12

14th November 2007

FIRST VERSION FOR 2008 RUNNING PERIOD

Object 4, Index 20 (CB004) thru Index 31 (CB016)

Remove all entries for Indices 20 through 31. DSM count reduced from 16 to 4 for run 8

Object 8, Index 30 (ZD001)

Change index from 30 to 28. Crate positions ZD001 and ZD101 swapped with ZP001 and ZP002

25th November 2007

Object 1, Index 26 (EM201)

Removed registers 0, 1, 3 and 4 and renamed register 2 (J/Psi selection) to register 0

Object 2, Index 16 (BE102) thru Index 22 (EE102), and Index 33 (BE101)

Removed all entries for these DSMS because the new algorithms have no registers

Object 2, Indices 23 (EE001) to 31 (EE009)

Renamed 2 existing TP registers to new HT registers. Renamed last TP register to new bitmask register. NOTE: The bitmask register has a different name for each EE00X DSM, because each bitmask is independent of the others.

Object 5, Indices 16 (BW001) to 30 (BW015)

Renamed 2 existing TP registers to new HT registers. Renamed last TP register to new bitmask register. NOTE: The bitmask register has a different name for each BW00X DSM, because each bitmask is independent of the others.

Object 6, Indices 16 (BE001) to 30 (BE015)

Renamed 2 existing TP registers to new HT registers. Renamed last TP register to new bitmask register. NOTE: The bitmask register has a different name for each BE00X DSM, because each bitmask is independent of the others.

28th November 2007

Object 9, Index 2 (FE102)

Removed all registers for this DSM since it has been removed from the FPE crate

Object 10

Renamed from FPW to FMS

Object 1, Index 23 (LD301)

Changed the meaning of registers 0:2 and removed registers 3:5 for the 2008 dAu algorithm

Object 3, Indices 16 (MD001) to 18 (MD002)

Added the second register and changed the meaning to TAC window edges instead of ADC thresholds/