ELSEVIER

Nuclear Instruments and Methods in Physics Research A 439 (2000) 418–426

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

www.elsevier.nl/locate/nima

A 240-channel thick film multi-chip module for readout of silicon drift detectors

STAR-SVT Collaboration

D. Lynn[a,*], R. Bellwied[b], R. Beuttenmueller[a], H. Caines[c], W. Chen[a], D. DiMassimo[a], H. Dyke[c], D. Elliott[a], M. Grau[a], G.W. Hoffmann[d], T. Humanic[c], P. Jensen[d], S.A. Kleinfelder[e], I. Kotov[c], H.W. Kraner[a], P. Kuczewski[a], B. Leonhardt[a], Z. Li[a], C.J. Liaw[a], G. LoCurto[c], P. Middelkamp[a], R. Minor[b], N. Mazeh[b], S. Nehmeh[b], P. O'Conner[a], G. Ott[d], S.U. Pandey[b], C. Pruneau[b], D. Pinelli[a], V. Radeka[a], S. Rescia[a], V. Rykov[b], J. Schambach[d], J. Sedlmeir[a], J. Sheen[b], B. Soja[a], D. Stephani[a], E. Sugarbaker[c], J. Takahashi[f], K. Wilson[b]

[a] *Brookhaven National Laboratory, P.O. Box 5000, Building 510A, Upton, NY 11973, USA*
[b] *Wayne State University, USA*
[c] *Ohio State University, USA*
[d] *University of Texas, Austin, USA*
[e] *Lawrence Berkeley National Laboratory, USA*
[f] *University of Sao Paulo, USA*

Abstract

We have developed a thick film multi-chip module for readout of silicon drift (or low capacitance ~ 200 fF) detectors. Main elements of the module include a custom 16-channel NPN-BJT preamplifier-shaper (PASA) and a custom 16-channel CMOS Switched Capacitor Array (SCA). The primary design criteria of the module were the minimizations of the power (12 mW/channel), noise (ENC = 490 e^- rms), size (20.5 mm × 63 mm), and radiation length (1.4%). We will discuss various aspects of the PASA design, with emphasis on the preamplifier feedback network. The SCA is a modification of an integrated circuit that has been previously described [1]; its design features specific to its application in the SVT (Silicon Vertex Tracker in the STAR experiment at RHIC) will be discussed. The 240-channel multi-chip module is a circuit with five metal layers fabricated in thick film technology on a beryllia substrate and contains 35 custom and commercial integrated circuits. It has been recently integrated with silicon drift detectors in both a prototype system assembly for the SVT and a silicon drift array for the E896 experiment at the Alternating Gradient Synchrotron at the Brookhaven National Laboratory. We will discuss features of the module's design and fabrication, report the test results, and emphasize its performance both on the bench and under experimental conditions.

1. Introduction

We have designed and fabricated a 240-channel multi-chip module in thick film technology for

* Corresponding author. Tel.: +1-516-344-4560; fax: +1-516-344-4206.
E-mail address: lynn2@bnl.gov (D. Lynn)

0168-9002/00/$ - see front matter
PII: S0168-9002(99)00934-1

readout of the silicon drift detectors designed for the SVT (Silicon Vertex Tracker) for the STAR [2] experiment at the Brookhaven National Laboratory Relativistic Heavy Ion Collider (RHIC). Parameters of the drift detectors relevant to the module design are their anode pitch (250 μm), low anode capacitance ($\sim$200 fF), low anode leakage current (generally $<$150 nA and typically $\sim$10 nA), and signal (gaussian-like current pulse, $\sigma = 20$–60 ns; integrated charge $\sim$20 000–300 000 e^-). We have designed and built a custom preamplifier-shaper integrated circuit matched to these parameters. Additionally, a switched capacitor array (SCA) integrated circuit, similar to previous designs [1], has been designed for our module. The SCA provides analog storage of the PASA output waveform. Each PASA and SCA contains 16 channels. Thus, the module contains 15 of each in order to provide the necessary 240-channel readout. The small space allocated to the module circuit (60 mm × 20.5 mm) requires that these integrated circuits be used in bare die form. The resulting high density and large number (30) of custom bare die used on the circuit present significant challenges with regard to module design, yield, and testing.

In the present paper we will first discuss various details of the PASA design, in particular the preamplifier feedback network. We then provide a functional description of the SCA and mention those features specific to the SVT version of the SCA. Details of the multi-chip circuit design, implementation in thick film technology, fabrication, and testing will be presented. Finally, we present performance results of the module, alone and integrated with the STAR drift detectors. The multi-chip modules have been integrated with drift detectors both in a system test and in a silicon drift detector array operated in experimental conditions in a heavy ion fixed target experiment (E896) at the Brookhaven National Laboratory Alternating Gradient Syncrotron (AGS). A photograph of the SVT multi-chip module is shown in Fig. 1.

2. Preamplifier-shaper

The preamplifier-shaper is a 16-channel integrated circuit (designed by D. DiMassimo) fabricated by Maxim (Oregon) in their SHPi NPN-BJT process. The SHPi process is a modern high speed, oxide isolated, bipolar process. It features small feature sizes (1.3 μm effective minimum emitter width, 0.7 μm minimum drawn emitter width), double layer metal, and high f_t at low currents (8.5 GHz at 0.5 mA). Additional features include high breakdown voltage ($LV_{CEO} = 8$ V), implanted and nickel-chrome resistors, low device junction capacitances (e.g. collector–substrate capacitance $C_{JC} \sim 34$ fF) and excellent current gain for small devices ($\beta_f \sim 100$).

The PASA is designed to amplify and shape current signals generated in silicon drift detectors from charged particles produced in heavy ion collisions. For particle identification at low momenta (and thus large dE/dx), the PASA must have a large dynamic range. Thus in addition to the usual requirements of low noise and power, the PASA must provide charge and timing information for input current signals with Gaussian widths $\sim$20–60 ns over a range of amplitudes of 20 000–250 000 signal electrons. To accommodate potentially high occupancy rates in the inner barrel of the SVT, a bipolar shaping function was chosen to prevent baseline shifts. Table 1 lists the main features and parameters of the PASA, and Fig. 2 shows the bipolar response function to a hit produced in the heavy ion experiment E896 at the AGS. The data in Fig. 2 is fit with the theoretical PASA response function (smooth line).

A schematic of one channel of the PASA is shown in Fig. 3. The input consists of two cascaded differential amplifiers with RC feedback. The main design issues of the preamplifier concern the RC feedback network. Some previous preamplifier designs have used external feedback resistors to achieve the high ohmic values necessary to minimize the resistor thermal noise. In our case where high-density multi-channel preamplifiers are required, the resistor must be integrated in the IC design and its value is limited by considerations of available real estate and the resistor distributed capacitance. Maxim provides implanted resistor simulation models that accurately describe the total value of the distributed capacitance. However, for large resistor values, the model (consisting of a lumped resistor shunted to ground at each end by

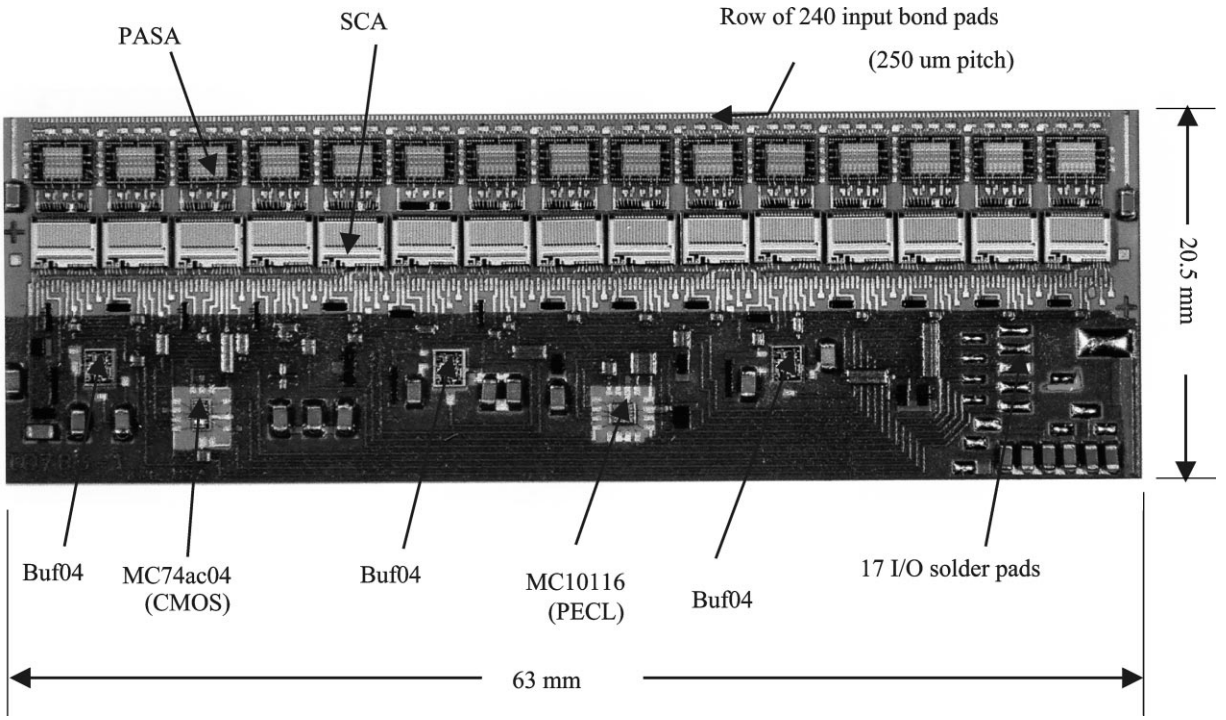

Fig. 1. Photograph of the multi-chip module.

Table 1
PASA specifications and performance

PASA parameters/specifications	
Technology	Maxim SHPi NPN-BJT process
Die size	3.3 mm × 2.4 mm
No. channels	16
Power dissipation	3.8 mW/Channel
Gain	7.2 μV/e$^-$
Noise ($C_{in} < 0.2$ pF)	ENC = 380 e$^-$ rms
Peaking time (10–100%)	50 ns
Dynamic range	2 V (275k e$^-$)
Linearity	$< 0.65\%$ ($Q_{in} < 20$ fC)
Crosstalk	$< 1\%$
Transfer function	$H(s) = ks/((s + 1/\tau_1)^5(s + 1/\tau_2))$
(Bipolar shaping)	$\tau_1 \approx 11$ ns, $\tau_2 \approx 500$ ns, k is a constant
Other features	• Zero gain at DC current • Optional DC gain = 0.6 mV/nA, for in situ leakage current measurements • Three gain settings: 1×, 1.5×, 2×

a capacitor with one half the value of the distributed capacitance) does not accurately describe circuit behavior. Considerable effort was spent to develop and verify simulation models of the large resistors, taking into account the distributed capacitance of the diffused resistors. Two main points emerged from this effort. First, at high frequencies the distributed capacitance serves to

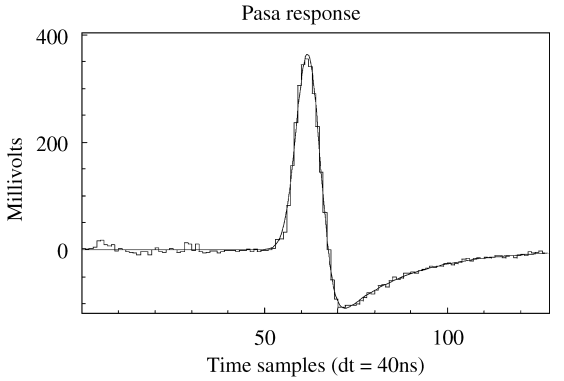

Fig. 2. PASA bipolar response to a signal produced in a silicon drift detector during a heavy ion experiment. The smooth line represents a fit of the theoretical PASA response function to the histogrammed data.

"short" resistor segments (in a distributed model) to AC ground, resulting in a lower effective feedback resistance. A higher thermal noise contribution at high frequencies results from this lower effective resistance. It is found that at resistor values higher than 250 kΩ the simulated noise contribution begins to differ from that calculated for a lumped resistor, and the noise only slightly decreases with increased resistor value. An independent analytic calculation agreed with the simulated result [3]. This analysis lead to the 250 kΩ value selected for the feedback resistor. The second point is that the distributed resistor capacitance introduces an additional phase lag that reduces the phase margin of the feedback circuit loop. By splitting the resistor into two sections (R_{f1} and R_{f2}) and adding a capacitor in parallel to each of them (C_{f1} and C_{f2}), the phase lag is decreased and the stability of the circuit with respect to a single feedback capacitor is improved. An additional advantage is an improved noise performance by reducing the parallel noise of the diffused feedback resistor in the frequency range of interest. One result of this careful modeling was that the initial production of the PASA performed as expected and required no design iterations.

The PASA requires three external voltage supplies, V_{dd1} and V_{dd2} (nominally 5 V) and V_{ee} (nominally -2 V). V_{cc} is internally derived from V_{dd1} to supply the first differential amplifier stage, isolating its supply from the remaining circuit. V_a is derived from V_{dd1} to bias the various transistor current sources that, for example, set the operating current in the differential amplifiers.

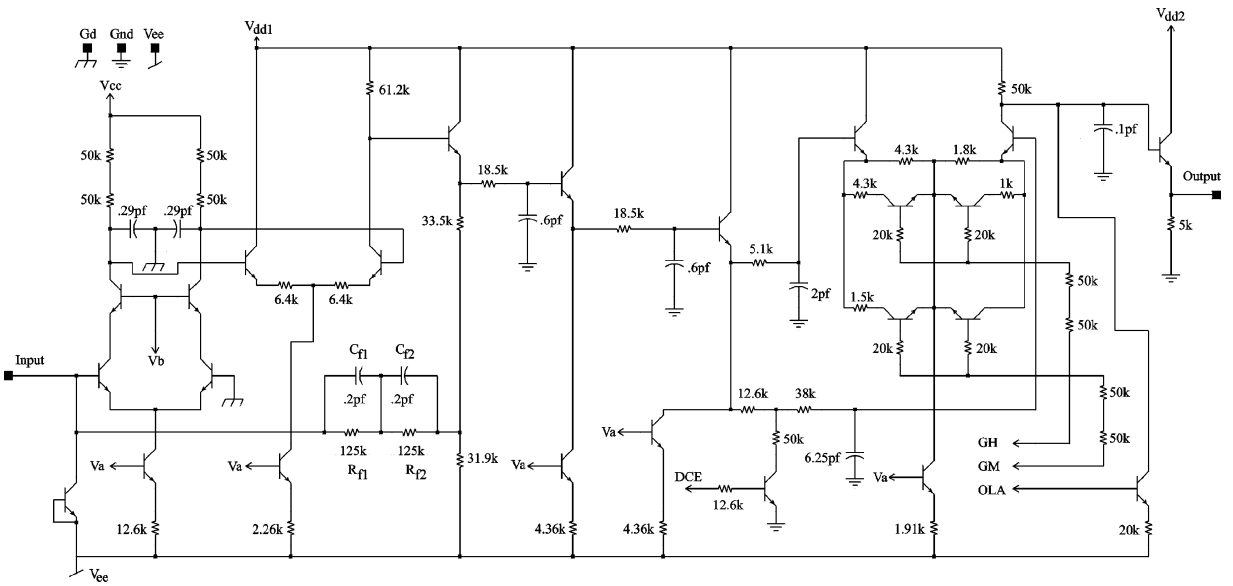

Fig. 3. Schematic of one PASA channel.

The shaper consists of two buffered RC stages (poles at τ_1; see transfer function in Table 1) followed by a differential amplifier. The buffered output of the second RC stage is fed to both ends of the differential amplifier but through different RC stages, resulting in an additional pole at τ_1 and τ_2 and zero gain at DC current. The AC gain of the differential amplifier, nominally 7 $\mu V/e^-$, may be set to 1.5 or 2 times nominal gain by applying a voltage to external pins GH (Gain High; see Fig. 2) or GM (Gain Max), respectively. These options are not utilized in the current module. Additionally, by externally supplying a voltage to DCE (Direct Current Enable; see Fig. 2), the associated transistor (with DCE driving its base) is driven into saturation. The voltage divider formed by the 50 kΩ resistor at the collector and the nearby 12.6 kΩ resistor result in different DC voltage levels at the two inputs to the final stage differential amplifier. This gives an overall gain of about 0.6 mV/nA at DC input current. This option (implemented in the current module) permits one to measure the leakage current from the drift detectors during calibration runs and thus track detector currents over time. The final stage of the PASA consists of an emitter follower driver biased with its own isolated supply, V_{dd2}, to decouple the large swings in output voltage and current from the more sensitive parts of the circuit.

We have analytically estimated the noise of the PASA and compared the result to simulation and measurement. Consideration of the main sources of parallel noise (feedback resistor, base currents of the first differential amplifier stage, and detector current) and series noise (R_{bb} and collector currents of first differential stage) predict a value of ENC = 310 e^- rms at zero input capacitance and ENC = 320 e^- rms at an estimated input capacitance of 0.2 pF (with bonded detector and 10 nA detector anode current), which are in reasonable agreement with the measured values of 350 e^- rms and 375 e^- rms, respectively. The simulation was more pessimistic, predicting ENC = 400 e^- rms at 0.2 pF.

3. Switched capacitor array

The switched capacitor array (designed by S. Kleinfelder) is a 16-channel analog memory storage device used to sample and store the output waveform from the PASA. It is fabricated in Orbit's 1.2 μm CMOS process. A simplified schematic showing one channel of both the SCA and PASA is shown in Fig. 4. Each channel of the SCA contains 128 capacitors on a common bus. The SCA operates in two modes, "acquire" and "read". During acquire mode the inputs of the SCA connect to the capacitor bus. At a frequency determined by an

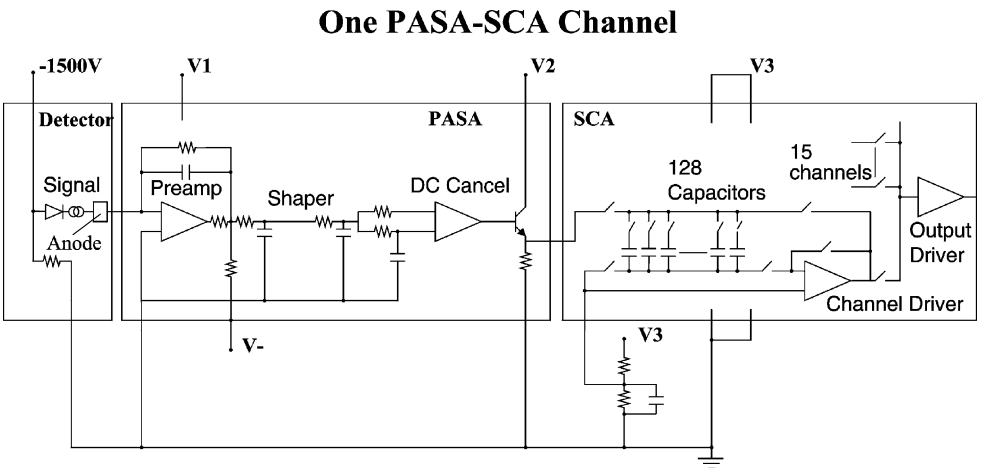

Fig. 4. Simplified schematic of one PASA-SCA channel.

Table 2
SCA specifications and performance

SCA parameters/specifications	
Technology	Orbit 1.2 μm CMOS
Die size	3.8 mm × 2.8 mm
No. channels	16
No. capacitors/channel	128
Power dissipation	6 mW/channel
Noise	2.2 mV (ENC = 300 e^- rms)
Gain	0.96–0.98 V_{out}/V_{in}
Crosstalk	$< 2\%$
Max readout clock frequency	2.4 MHz
Typical acquire clock freq.	25 MHz

externally provided differential clock (25 MHz in our implementation) the capacitors sequentially connect to the bus and sample the input voltage. After 128 capacitors have sampled the input an internal counter resets, and sampling continues, overwriting previously stored values. Upon receipt of a trigger the SCA is placed in read mode, which disconnects the input from the capacitor bus and connects the bus to that channel's opamp driver. A token passing scheme multiplexes sequentially each channel's output onto the SCA's common output driver at a frequency of about 2.2 MHz (in our implementation). The same token passing scheme permits the multiplexing of an arbitrary number of SCA analog outputs onto a common bus. Table 2 lists the parameters describing the SCA and its performance.

4. Multi-chip module

The multi-chip module is a high-density custom thick film hybrid circuit containing 35 integrated circuits. Its longitudinal dimension of 63 mm corresponds to the size of the SVT silicon drift detectors. Its length of 20.5 mm in the other direction is limited by the physical constraints of the SVT barrel geometry. The circuit is fabricated on a 0.65 mm thick beryllia substrate chosen for its long radiation length and good thermal conductivity. Table 3 summarizes the main module parameters and specifications.

Table 3
Multi-chip module specifications and performance

Multi-chip module parameters/specifications	
Technology	Thick film on beryllia substrate Dupont QM silver-based pastes
Min. feature size	150 μm lines/spaces
Size	63 mm × 20.5 mm
No. channels	240
No. time samples	128/channel
Total no. "pixels"	128 × 240 = 30 720
Components	30 custom-integrated circuits 5 commercial ICs 56 thick film resistors 21 surface mount capacitors
Sampling rate	25 MHz 128/25 MHz = 5.1 μs ≈ drift time
Readout rate	2 MHz Total time = 128 × 80/2 MHz = 5 ms
Power supplies	V1 5 V (PASA) V2 5 V (PASA) V3 5 V (SCA, 10116, 74AC04) V^- −2 V (PASA) ± 6 V (Buf04)
Power dissipation	12 mW/channel = 2.9 w
Noise	ENC = 490 e^- rms (no detector) ENC = 530 e^- (with biased detector)
Radiation length	1.4%

The circuit contains 5 main metal planes and requires approximately 20 masks and fabrication steps. The first metal plane is a ground plane covering almost the full extent of the beryllia substrate. Next are two planes to provide power to the integrated circuits. Two layers of signal and power traces are then used to interconnect the various components.

Dupont QM silver based pastes are used in the thick film fabrication of the circuit. Noteworthy is our use of QM-14 silver paste for the ground and power planes. This paste is designed for inner layer conductors and has a very low resistance of $\sim 2\ m\Omega/\square$ at a typical fired thickness of 15 μm. Typical thick film conductor pastes have 5–10 times higher resistivities at the same fired thickness. The use of the QM-14 silver paste results in a much lower radiation length contribution for similar voltage drops across the power and ground planes. Palladium–silver is used for the trace layers where

minimum line widths and spaces of 150 μm are maintained.

The PASAs are located at a 4 mm pitch along the row of 240 module input pads (see Fig. 1) and have their channel inputs bonded to the pads. Connection to the drift detector anodes are made via a second wire bond from the module input pads to the anodes. Although this scheme adds slightly higher noise than one where the PASA inputs are bonded directly to the anodes (the PASA-to-module pad bond wire increases the overall ENC by about 30 e^- rms), this scheme simplifies the assembly and detector-to-module wire bonding. Similarly the SCAs are placed at a 4 mm pitch and have their channel inputs bonded directly to the PASA channel outputs in order to conserve module real estate.

The 15 SCAs are grouped into three chains of 5 SCAs, each chain having a common multiplexed output. Thus there are three analog signals per module which must be driven off the module for digitization. Three Analog Devices Buf04 unity gain drivers are used for this purpose. The level of multiplexing was determined by the required maximum total readout time of about 5 ms (STAR requirement) and the maximum SCA readout frequency of about 2.4 MHz (80 channels × 128 time samples/2.4 MHz ∼ 4–5 ms). The SCA requires a differential clock signal that is used for both the readout mode and acquire mode clocking. This clock is provided externally and fanned out into three clock signals by an ECL triple line receiver/driver operated at pseudo-ECL (PECL) levels. Each clock supplies a chain of five SCAs. Additional externally provided control signals to the SCA are fanned out to all 15 SCAs by a CMOS hex inverter. Due to the high-density of components on the module only a relatively small number of ceramic chip capacitors are used for high-frequency power supply decoupling. It is found that for proper module operation low-frequency tantalum capacitors are needed on the power supplies in close proximity to the module. Provisions for these capacitors exist in the SVT design. Connections for signals and power to the outside are made through soldered i/o pads. This permits a higher density of connections than is available with any commercial micro-miniature connector that we investigated.

The high number of custom-integrated circuits requires some consideration of yield and testing issues. The PASA has a production yield of about 70%, and the SCA a yield of about 50%. This production yield is the percentage of dice passing all wafer level tests. We further define a die assembly yield "y", which is the percentage of dice that passed the wafer level tests and then function correctly after mounting on the multi-chip module. The probability (module yield) that all of the 30 custom ICs function is y_{30} (we assume the same yield y for both the PASA and the SCA in this discussion). Even a high die assembly yield of $y = 98\%$ results in only an overall total module yield of 55%. Since the high density of ICs on the module make rework difficult and undesirable, the implications are the following. First, the wafer level probe station testing must be sufficiently rigourous to insure that all die passing the probe test are completely acceptable for the final module assembly. This necessitates full and rigourous AC testing of both the PASA and the SCA. Additionally, great care must be exercised in the subsequent sawing of the wafer and handling of the good dice to insure that less than 1% are subsequently damaged. This requires very careful handling techniques to avoid electrostatic discharge failures, as well as rejection of any die upon visual inspection that appears even potentially damaged. Such testing, inspection, and handling procedures have been implemented for our last two productions totaling approximately 58 modules, and resulted in an overall module yield of about 71%. This figure translates into an overall die assembly yield of about 99%. Module failure modes other than those failures due to bad dice have not been seen in our last two productions.

We mention one aspect of our die testing which is noteworthy. We originally constructed a probe card for the PASA testing which made contact with the PASA input pads to permit charge injection into the preamplifiers so that we could test the gain, linearity, and dynamic range of the PASAs. Immediately upon the unshielded probe pins contacting the input pads, however, the PASA outputs began to oscillate. The solution, which may be appropriate for other preamplifiers intended for low input capacitance, is to construct a probe card in which the input probe pins do not contact the

PASA inputs, but remain 25–50 μm above the PASA pads. The capacitance due to the proximity of the probe pins to the PASA inputs (we estimate about 2 fF) permits us to inject sufficient charge to test the PASA over its full dynamic range.

5. Results

We constructed a prototype system of the SVT consisting of four silicon drift detectors read out by eight modules. A batch of 14 modules were assembled, 10 of which fully functioned and satisfied all specifications (71% yield). The typical ENC associated with each pixel (i.e. a specific channel and SCA capacitor) was 490 e^- rms. After the modules were bonded to the drift detectors and the detectors were powered and depleted, the typical ENC increased to 510 e^- rms. The PASA and the SCA contribute most of the noise, with the external electronics responsible for only negligible increase. Fig. 5 shows the average channel pedestal and noise for one side (4 modules) of the system. The noise is uniform across the channels. Two channels were non-functioning (as seen in both the noise and channel plots) and one other channel had low gain (seen in the noise plot). This gives us a yield of good channels of 99.7%. The other four modules similarly had a yield better than 99.5%. Pulse injection via an x–y position controlled laser verified that all these anodes were functioning. A typical laser-generated signal (averaged over 100 events) read out through the module is shown in Fig. 6.

In addition, we recently installed a 15 plane assembly of silicon drift detectors in experiment E896

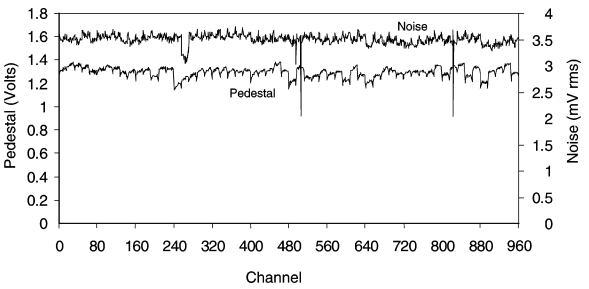

Fig. 5. Noise and pedestals for four multi-chip modules (960 channels) that read out one side of a four-detector system.

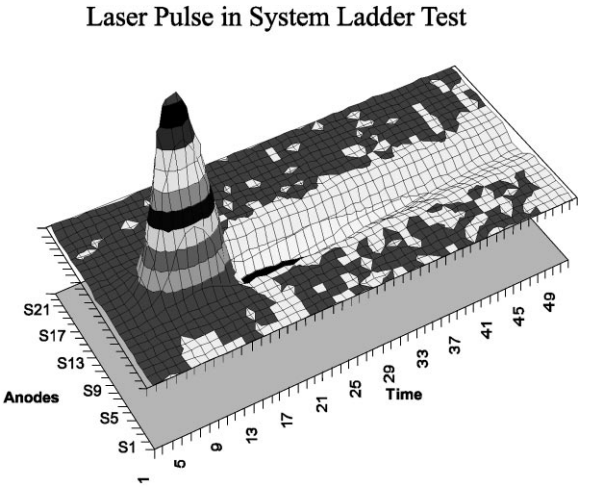

Fig. 6. Laser pulse signal read out from a silicon drift detector by a multi-chip module in the system test.

at the AGS. Each plane consisted of a printed circuit board mounted with one STAR-SVT silicon drift detector and two multi-chip modules. Though the analysis is still in its preliminary stage, all detectors and modules were measured to function properly. Each half-detector (corresponding to one module) saw an average of about 30 hits per event [4], a number comparable to the occupancy expected in the STAR experiment. Here we note that the percentage of functioning anodes was better than 98.5%, a figure that includes one PASA (16 channels) that was destroyed during detector-to-module wire bonding. The ENC was somewhat higher than in the system test, averaging about 760 e^- rms. We believe this increase is due primarily to a non-optimal powering scheme in which all the modules were run from common supplies. In the SVT power scheme no more than eight modules are powered from the same supplies. Nonetheless preliminary analysis demonstrates that minimum ionizing hits are readily seen and reconstructed above the noise.

6. Conclusions

We have designed and fabricated a 240-channel multi-chip module for readout of silicon drift

detectors. A 16-channel preamplifier-shaper and a 16-channel switched capacitor array have been designed and fabricated for the module. Both have functioned according to specifications. The multi-chip module design achieves low noise, low power, long radiation length, and high density. The last two production runs have resulted in about 41 working modules with an average yield of 71%. These modules have been successfully integrated with STAR-SVT silicon drift detectors in both a prototype SVT system test and in a 15-plane silicon drift detector array operated in a heavy ion experiment at the AGS. Signal from laser injection and from charged particles are easily seen, and good noise performance has been achieved.

Acknowledgements

This work is supported in part by the US Department of Energy (under contract No. DE-AC02-98CH10886) and DE-FQ02-92ER40713), the National Science Foundation (under grant PHY-9511850), and the Robert A. Welch Foundation.

References

[1] S.A. Kleinfelder, IEEE Trans. Nucl. Sci. NS-37 (1990) 1230.
[2] J.W. Harris, the STAR Collaboration, Nucl. Phys. A 566 (1994) 277c.
[3] S. Rescia, Brookhaven National Lab, to be published.
[4] J. Takahashi et al., Nucl. Instr. and Meth. A 439 (2000) 497.