Micro-vertex

Pixel Activities

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Introduction

- **Micro-Vertex detector development**
  - **Goals and Strategy**
    - **Funded project 2006 (preliminary proposal this Dec)**
    - **1ST Generation based on LEPSI/IReS MIMOSA-5 CHIP (slow read out)**
    - **2nd Generation fast readout – to be determined**
  - **Activities**
    - **Simulations**
    - **MIMOSA-5 readout**
    - **Advanced APS development**
    - **Mechanical**

Features

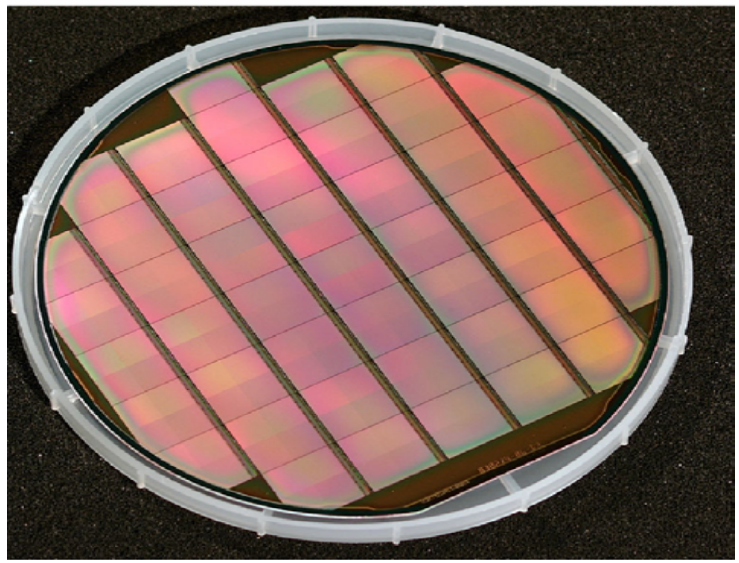
- 2 layers
- Inner radius ~1.8 cm
- Active length 20 cm
- Readout speed 20 ms (generation 1)
- Number of pixels 130 M

Simulations

- Original work of Retiere and Matis show substantial improvement in D meson statistics, simulations based on parameterized performance of STAR detectors
- Full tracking detailed simulations (Schweda and Retiere) awaiting tracking debug
  - Cut optimization
  - Refinement of detector requirements (pixel size)

MIMOSA-5 LEPSI/IReS chip readout

- MIMOSA-5, full wafer engineering run – significant readout infrastructure
- Test board development (Bieser and Gareus)
  - 2 by 2 cm MIMOSA-5 chip
  - LBNL development using 4 commercial 50 MHz 14 bit ADCs
- Considering piggy back readout chip design with CDS and signal scarification
  - Full frame by frame comparison for CDS, i.e. memory for frame storage and leakage current subtraction



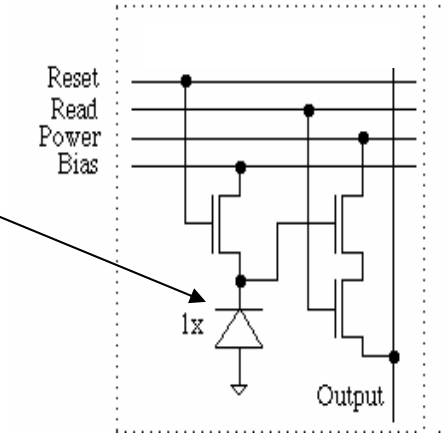
Advanced APS designs

- Goal, increase speed with on detector chip zero suppress and by avoiding full frame readout
- Requires improvements in signal to noise
  - Noise sources
    - KTC reset noise
    - Fixed pattern noise, threshold variation, leakage current variation
- Programs at LEPSI/IReS
- Programs at UCI/LBNL (Stuart Kleinfelder, Yandong Chen)
  - Photogates
  - CDS clamp circuit
  - Active Reset

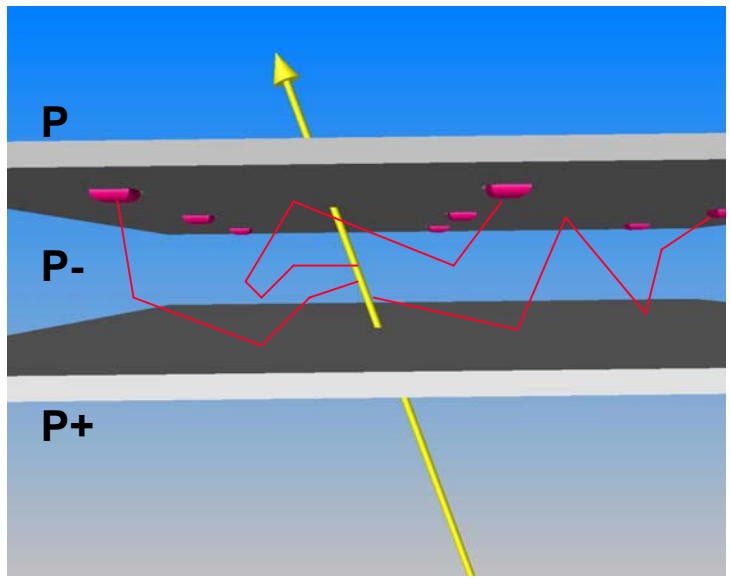
Photo gate purpose - addresses standard diode limitations

- CDS removal of fixed pattern noise and KTC reset noise on the chip (standard diode requires CDS off chip)

Standard APS diode structure



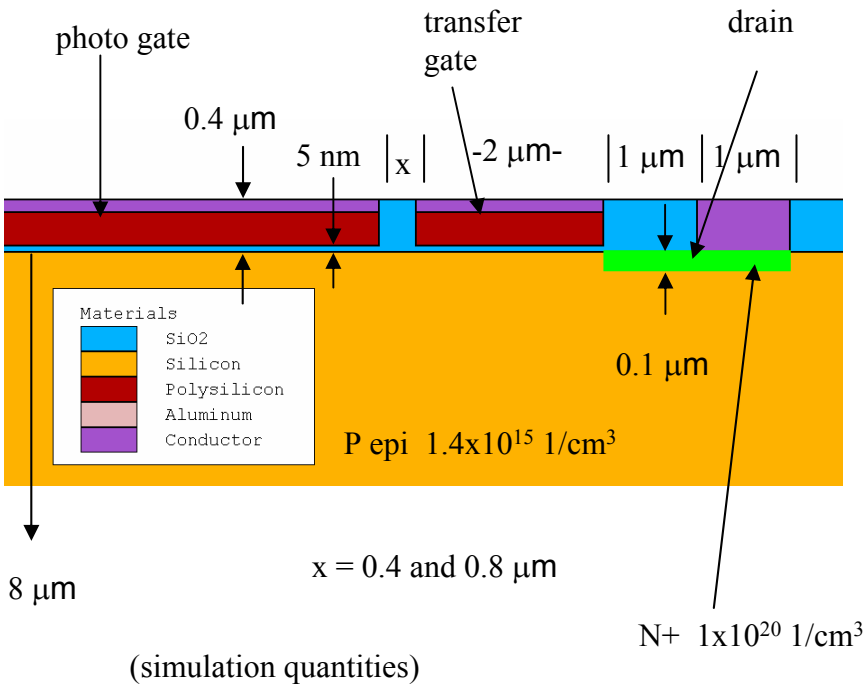
- Increase signal by reducing signal spreading to adjacent pixels. The photo gate permits large geometry without adding capacitance to the sense node.



Standard diode geometry

Photo-gate geometry

- **Large photo-gate to collect large fraction of the charge on a single pixel, directly on the p- epi layer**
- **Small transfer gate also directly on p- epi layer**
- **Small drain (minimum capacitance) connected to source follower gate (sense node)**



(simulation quantities)

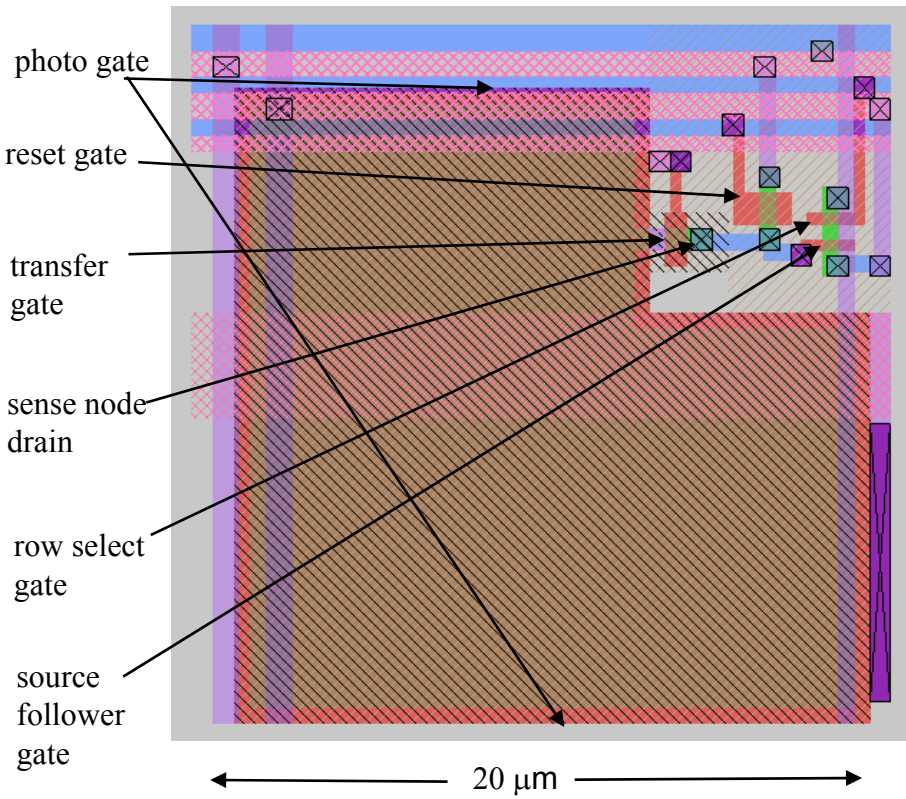
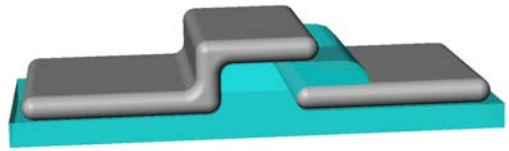


Photo-gate issues in standard CMOS

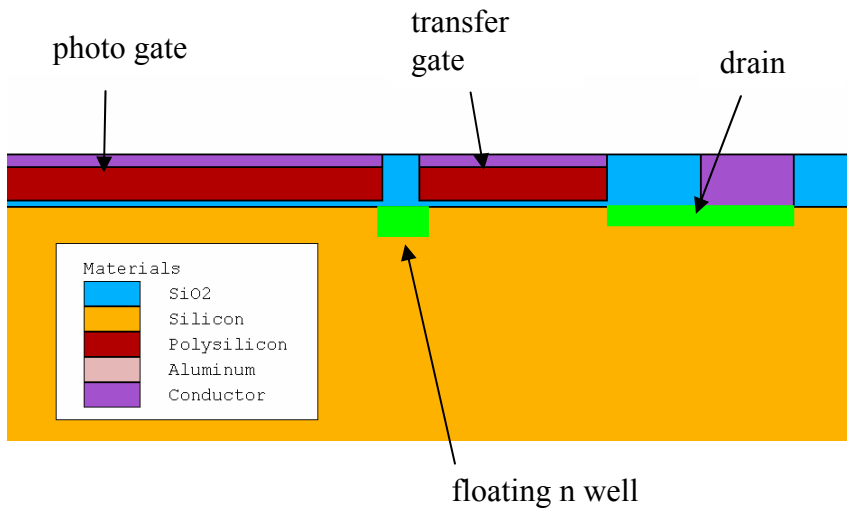
- **No double poly process – possible poor transfer between gates because of low transverse field**

double poly, standard for CCDs



single poly, limitation of CMOS

- **Floating n well between gates, a bad solution to the transfer problem with single poly**



- **Sub-micron process may solve problem**

Photo gate/transfer gate operation

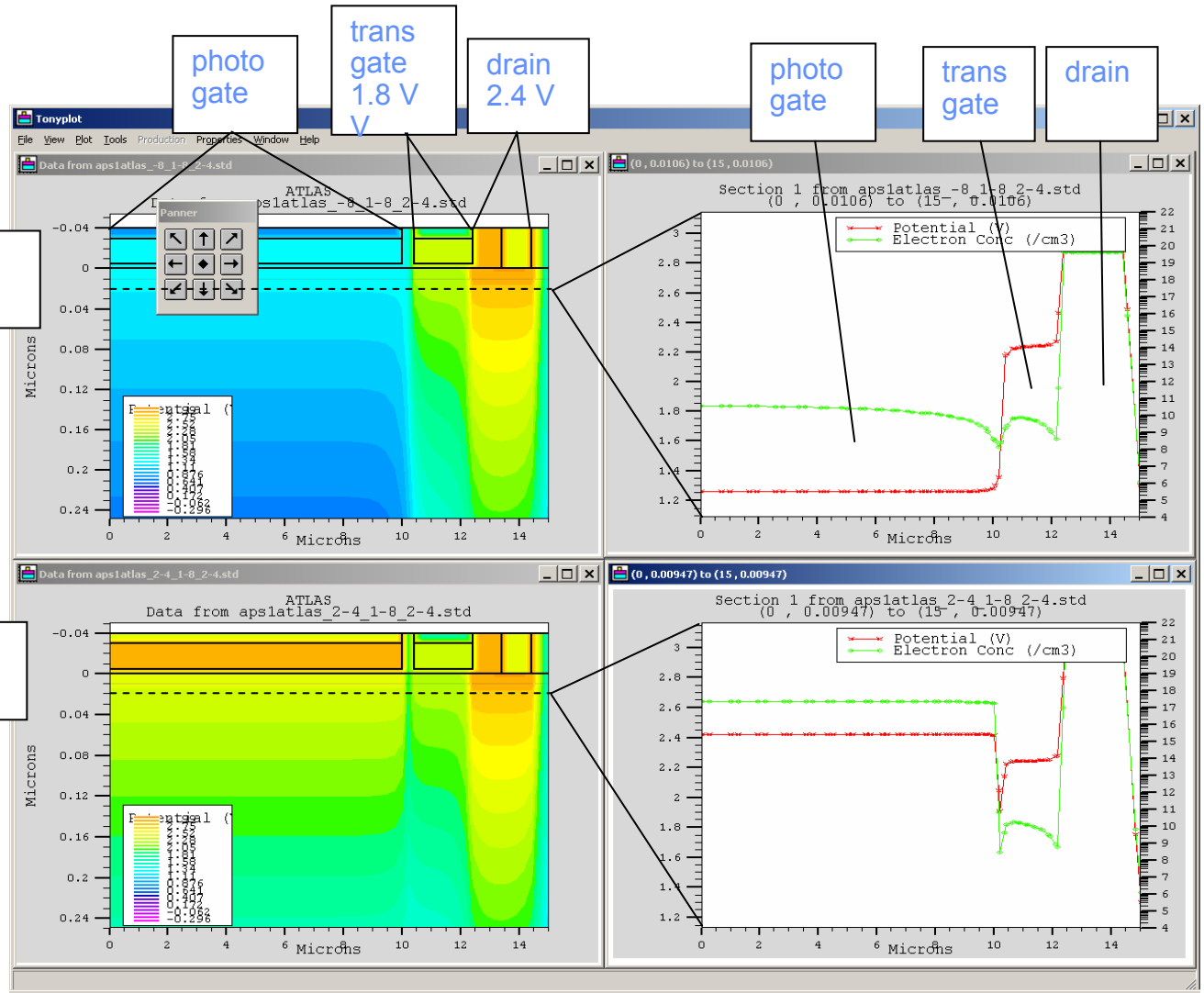
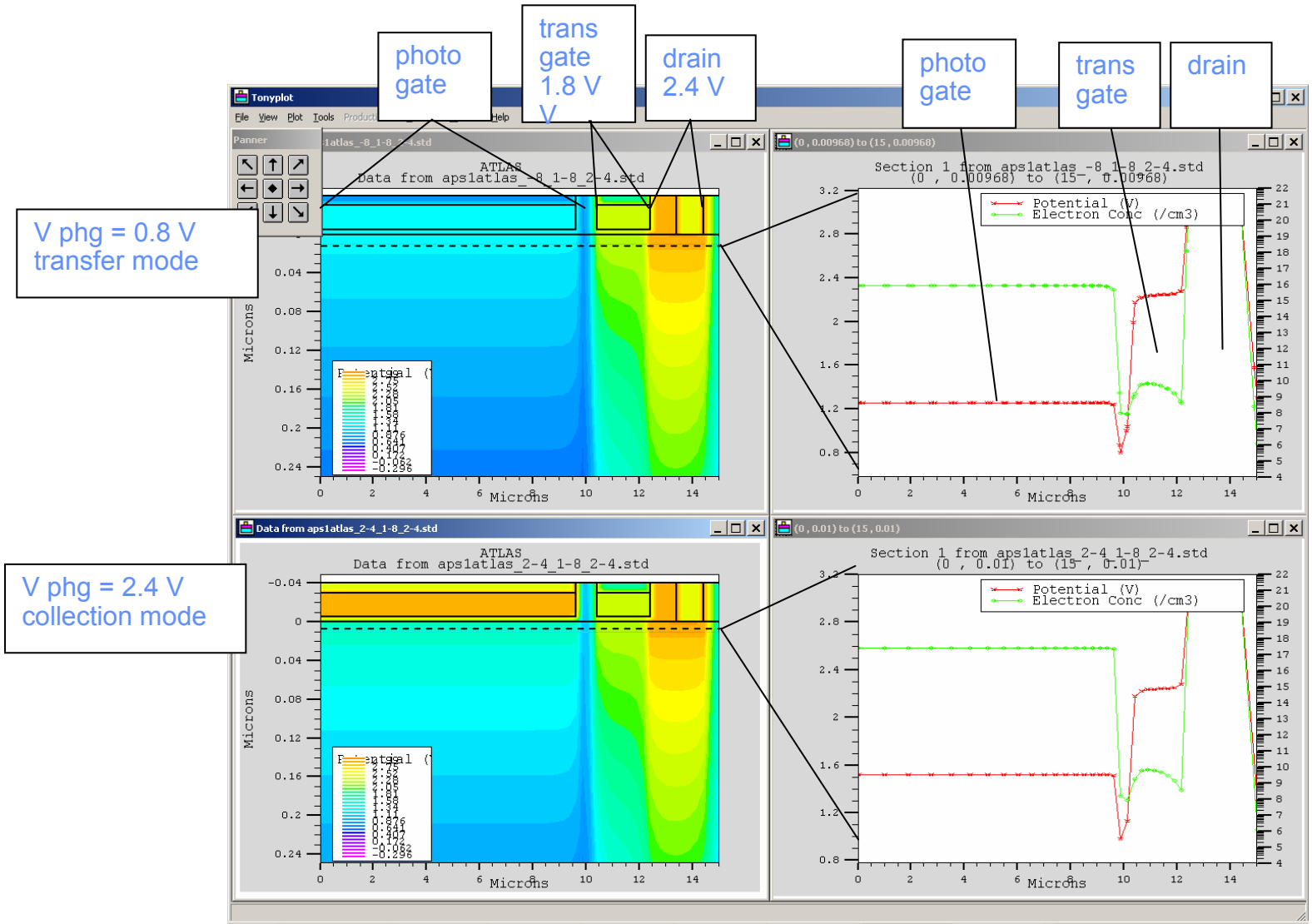


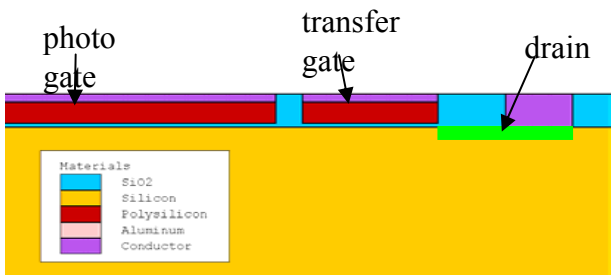
Photo gate/transfer gate with 800 nm separation

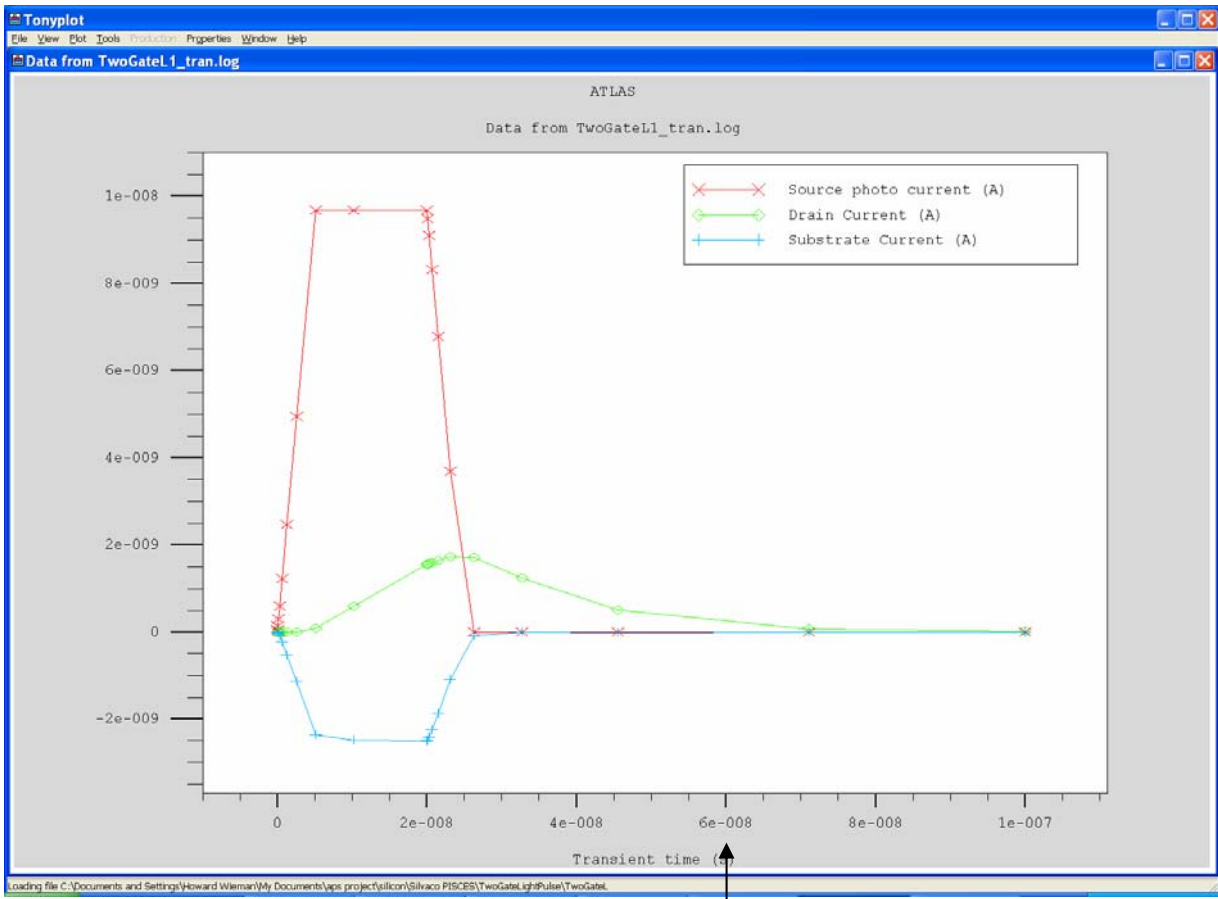


Drain current after light injection

- 400 nm between photo gate and transfer gate, no floating n well
- Nano amp drain current
- Rapid electron transfer - complete in 60 ns

Light injection

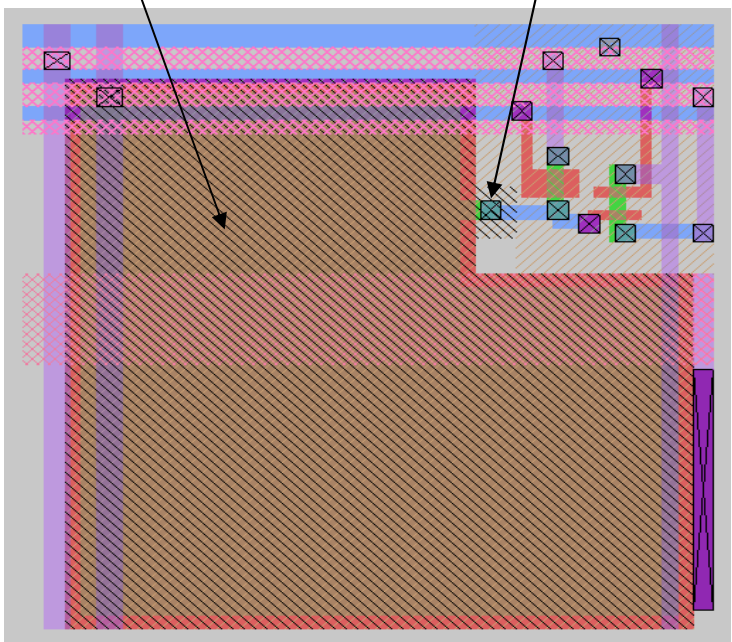




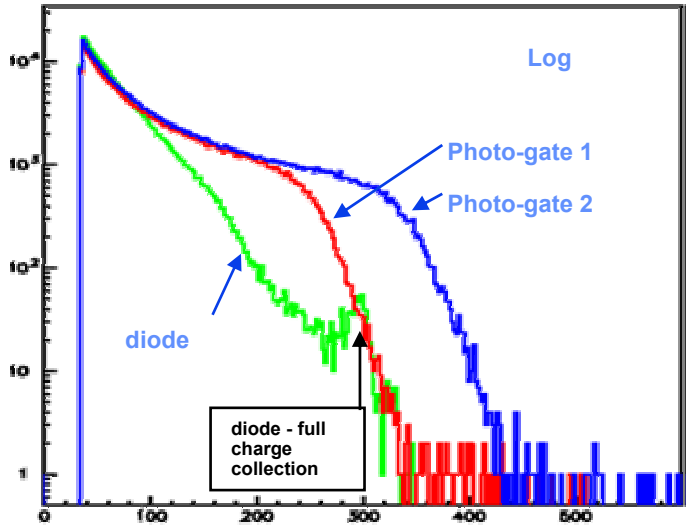
60 ns

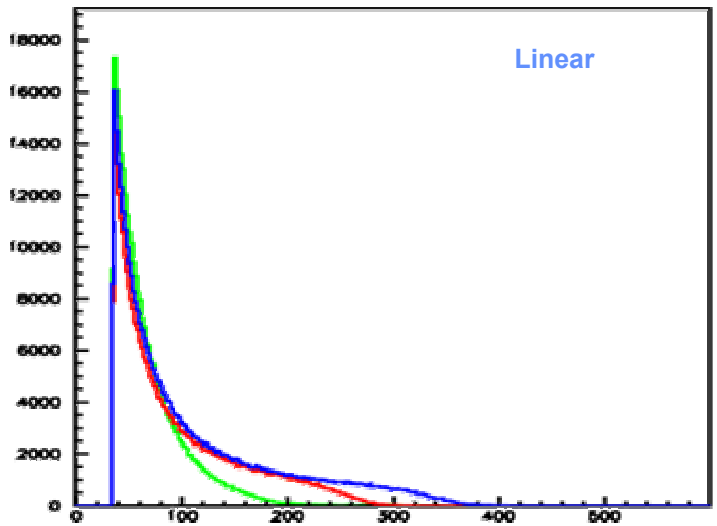
First silicon tests, comparing photo-gate with standard diode structure

Photo-gate directly to sense node drain



Output signal for Fe^{55} X-ray test





DC bias:
V photo-gate 0.6 V
V drain 2.4 V

Issue:

Why is the signal spread out – is it surface traps under the gate?

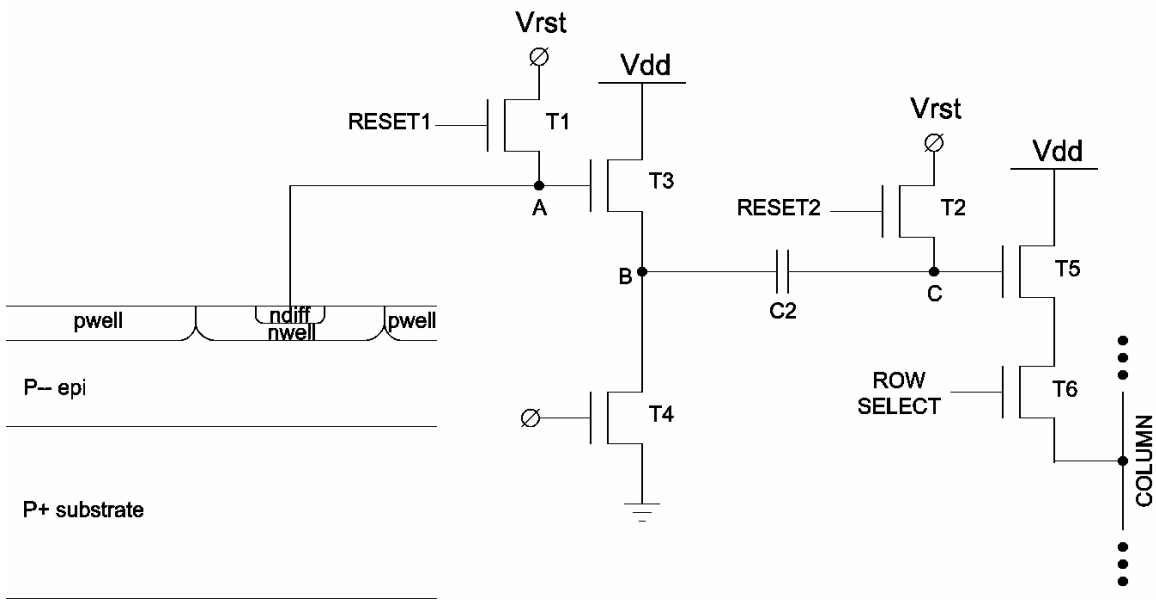
CDS clamp

- **kTC noise removed by clamp circuit – noise scales as**

$$\sqrt{kT/C_2}$$

Rather than

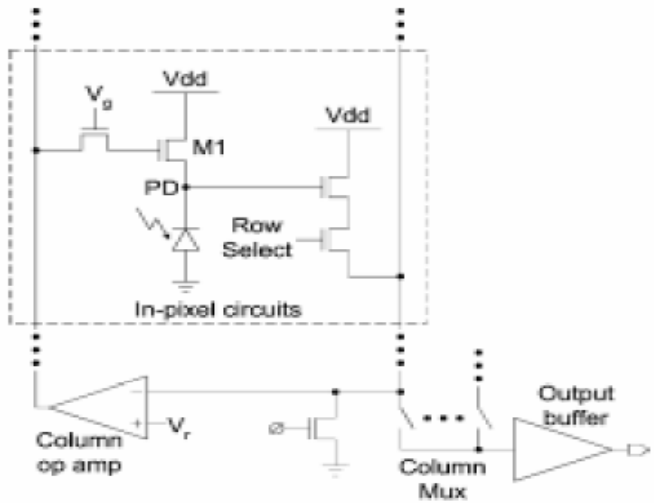
$$\sqrt{kTC_{diode}}$$



Active reset

- Signal from output is amplified to zero the input
- Inferred noise 5.1 electrons RMS as compared to kTC reset of 38 electrons RMS

Our standard APS gives
10 electrons RMS after CDS

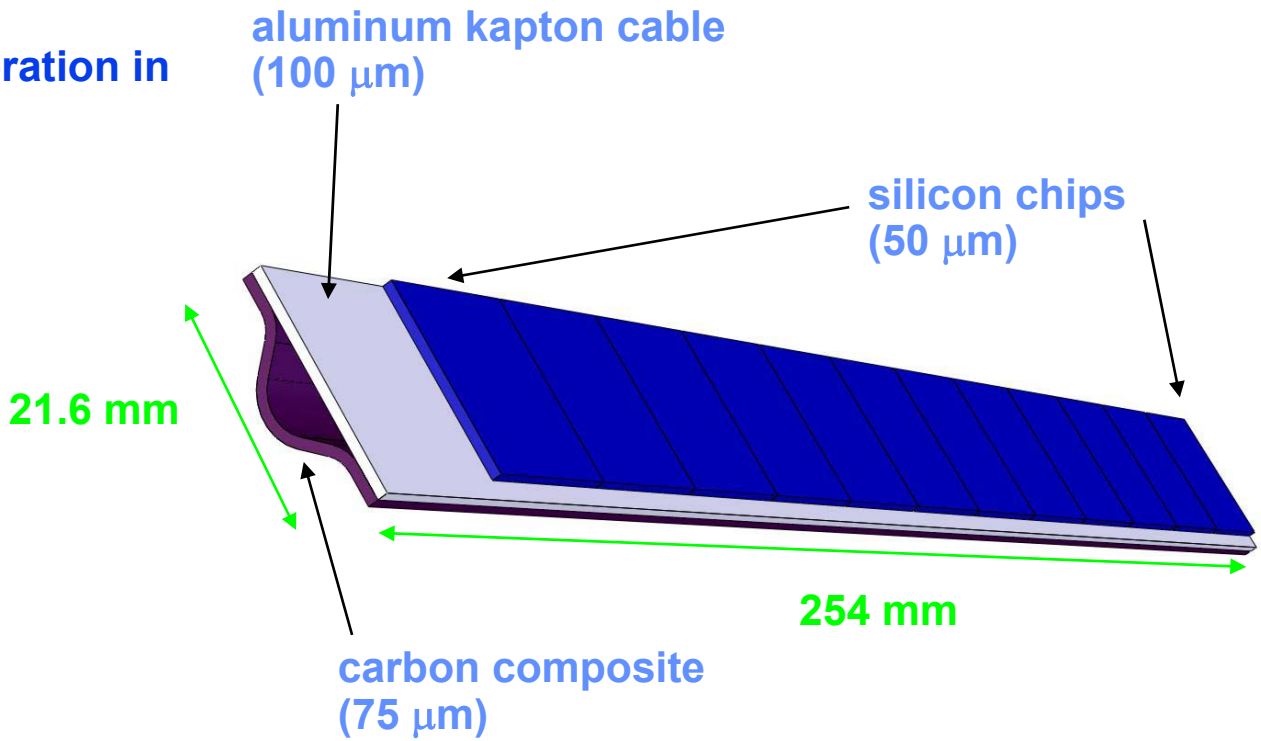


Mechanical

- Rapid insertion and removal for replacement and changing detector configuration
- Minimum thickness: 50 Micron Si Detector – 50 Micron Si Readout chip
- Air cooling
- Composite beam pipe?

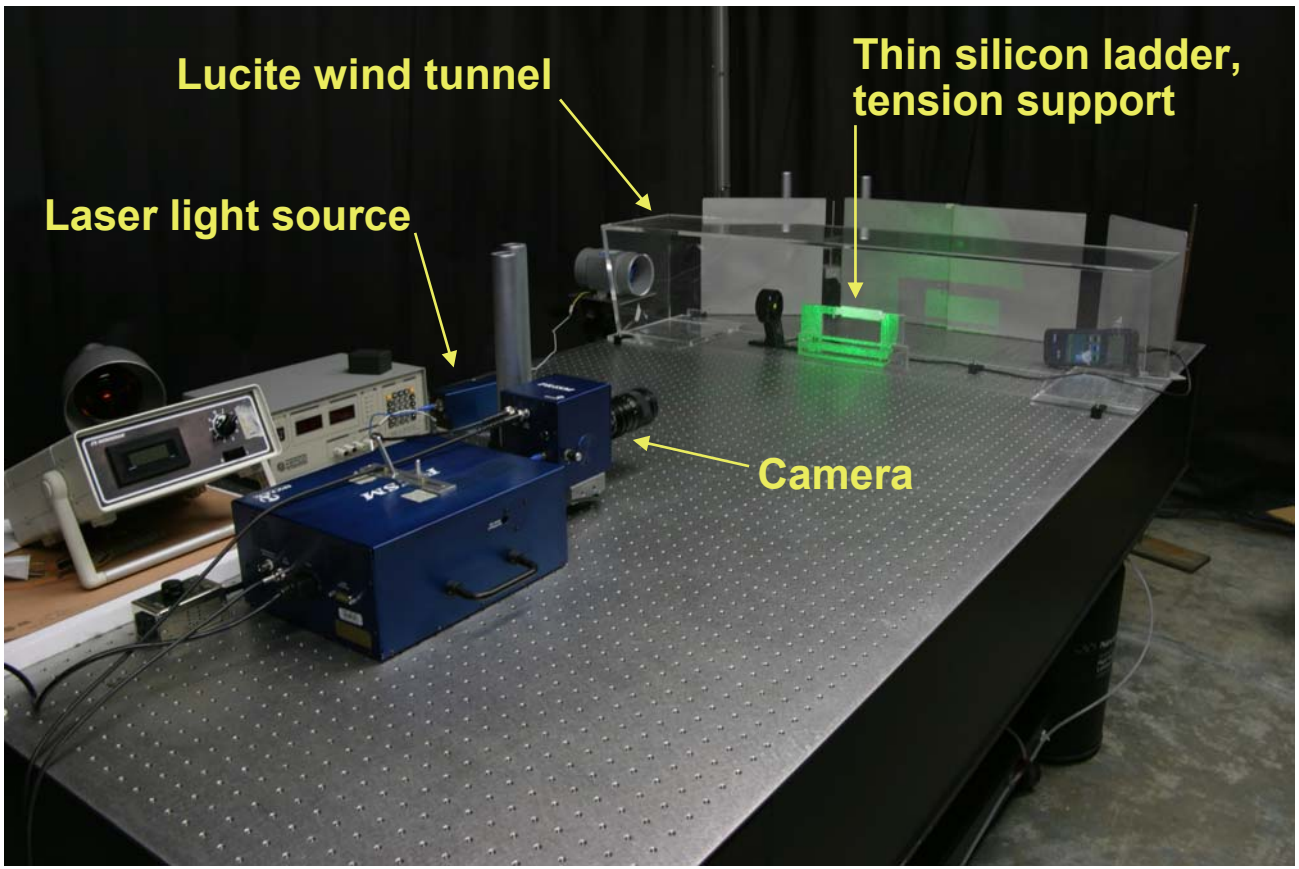
Thin stiff ladder concept

- Under construction
- Will be tested for vibration in our wind tunnel

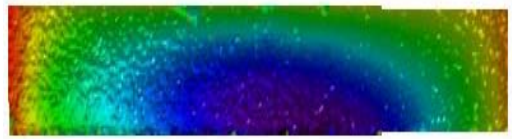


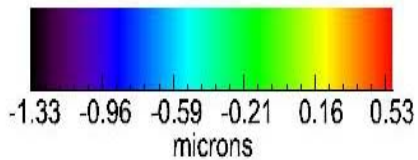
Air cooling and vibration

- 1-2 m/s air cools 100 mW/cm^2
- TV holography shows 2 μm vibration for tensioned silicon structure

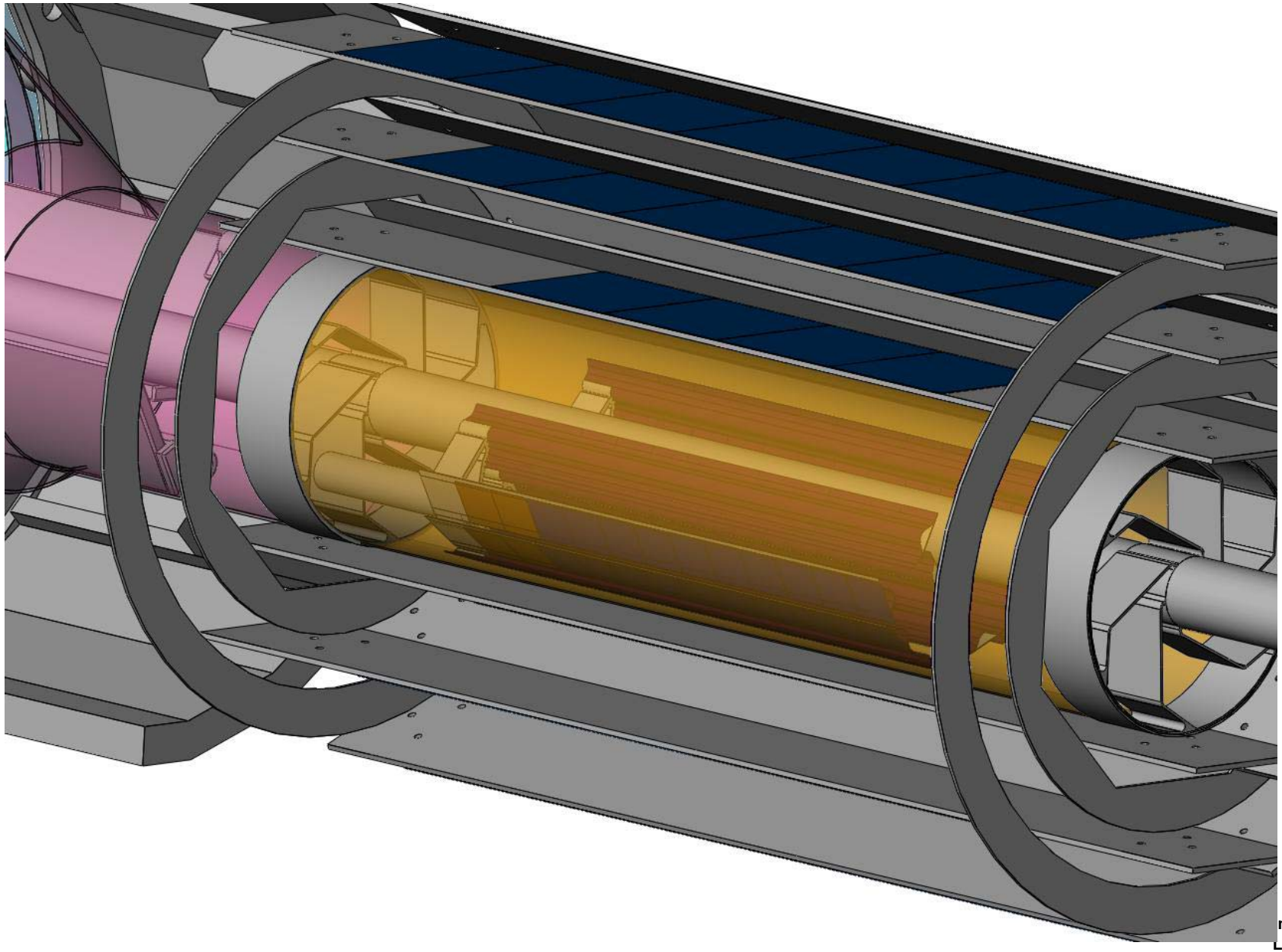


TV holography vibration map

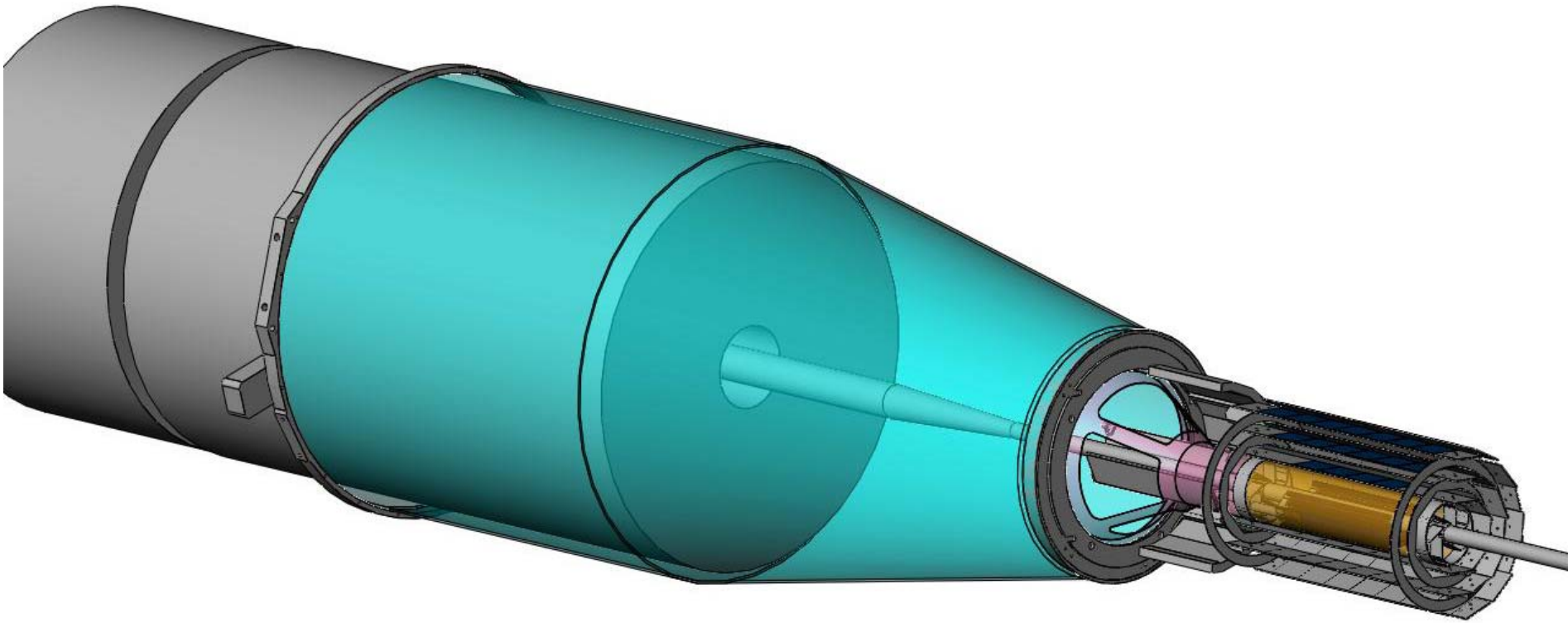




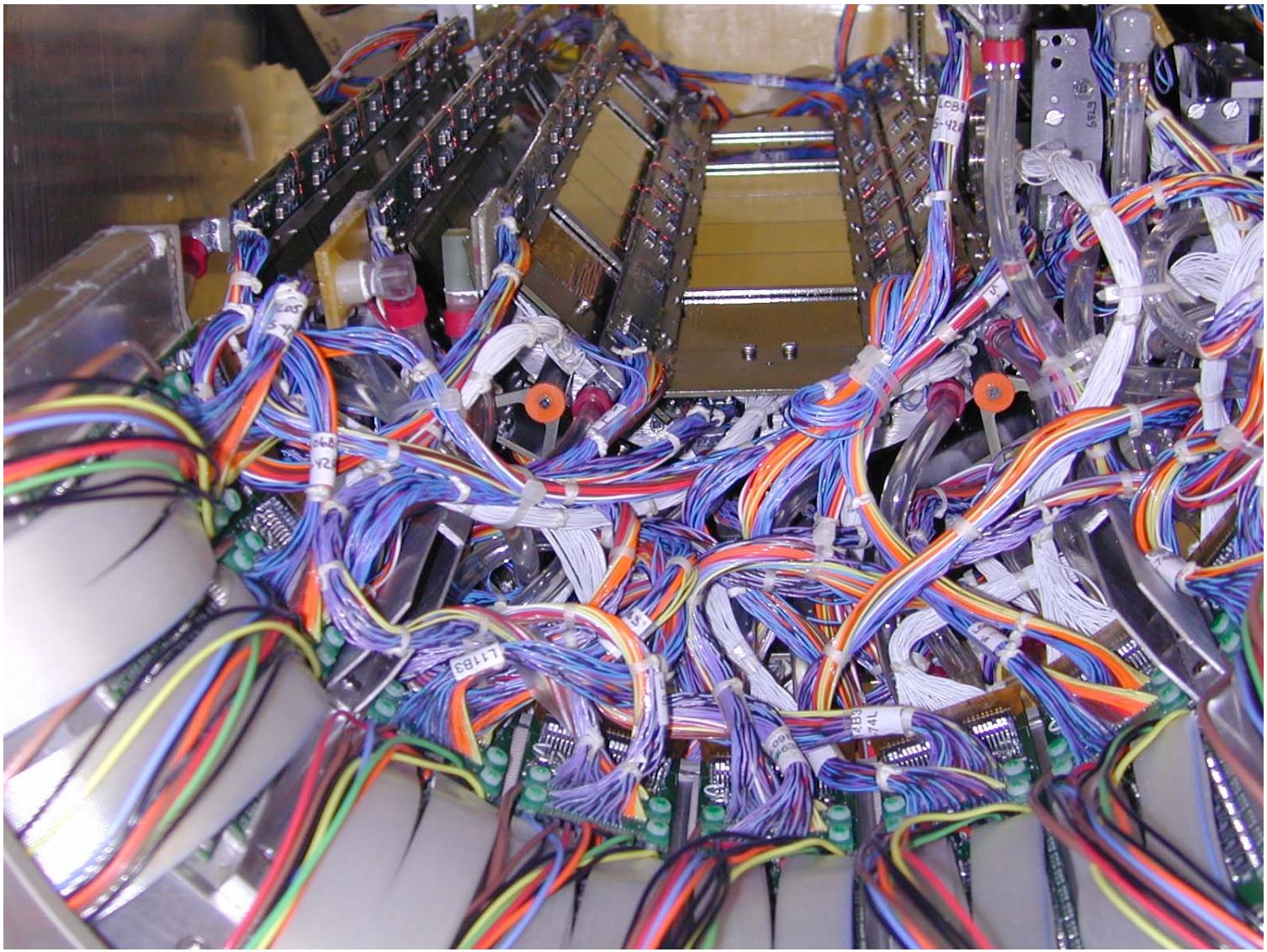
Inner STAR model – SVT and micro-vertex



STAR inner model – FTPC, SVT and micro vertex



The reality

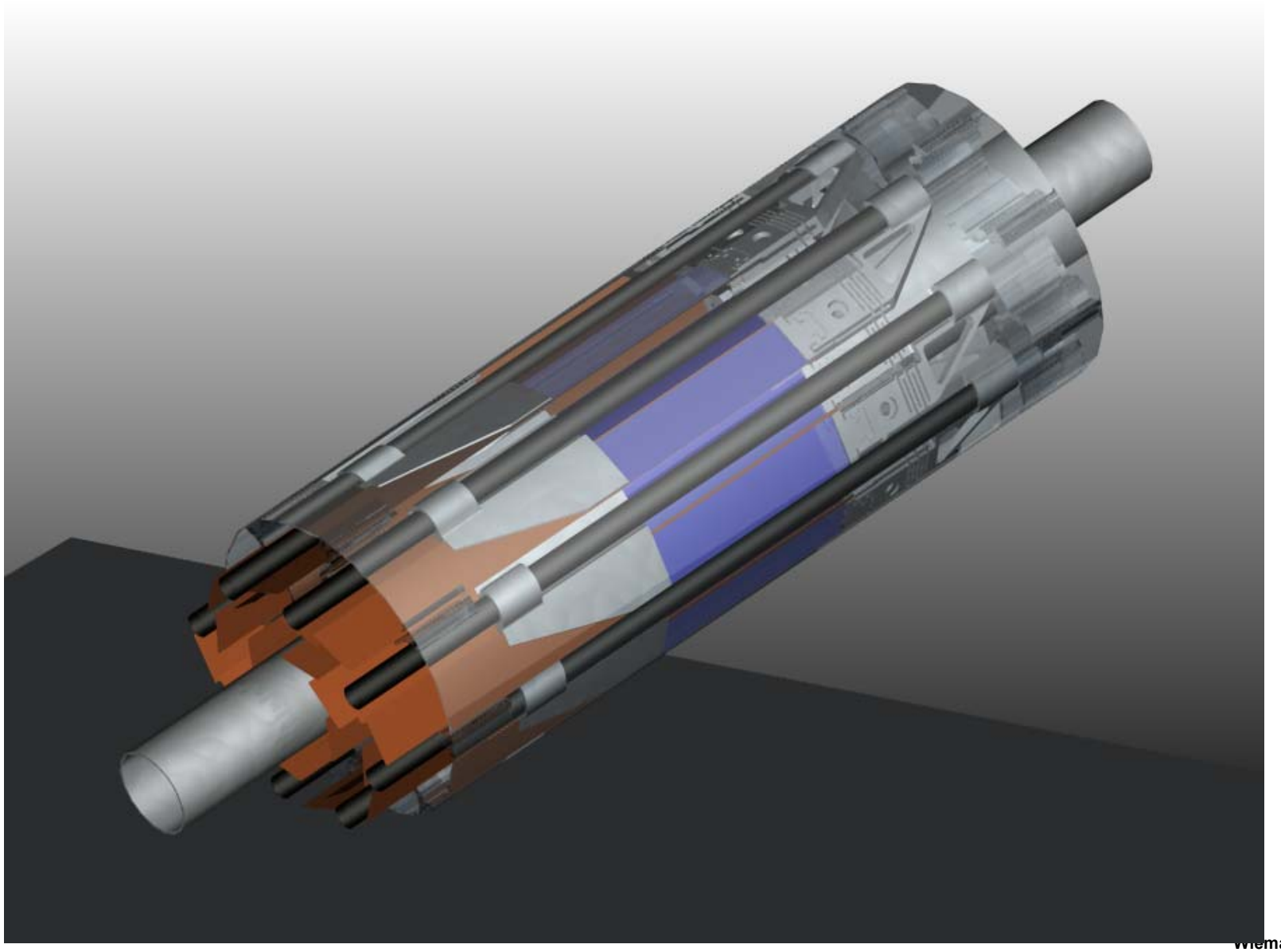


Conclusion

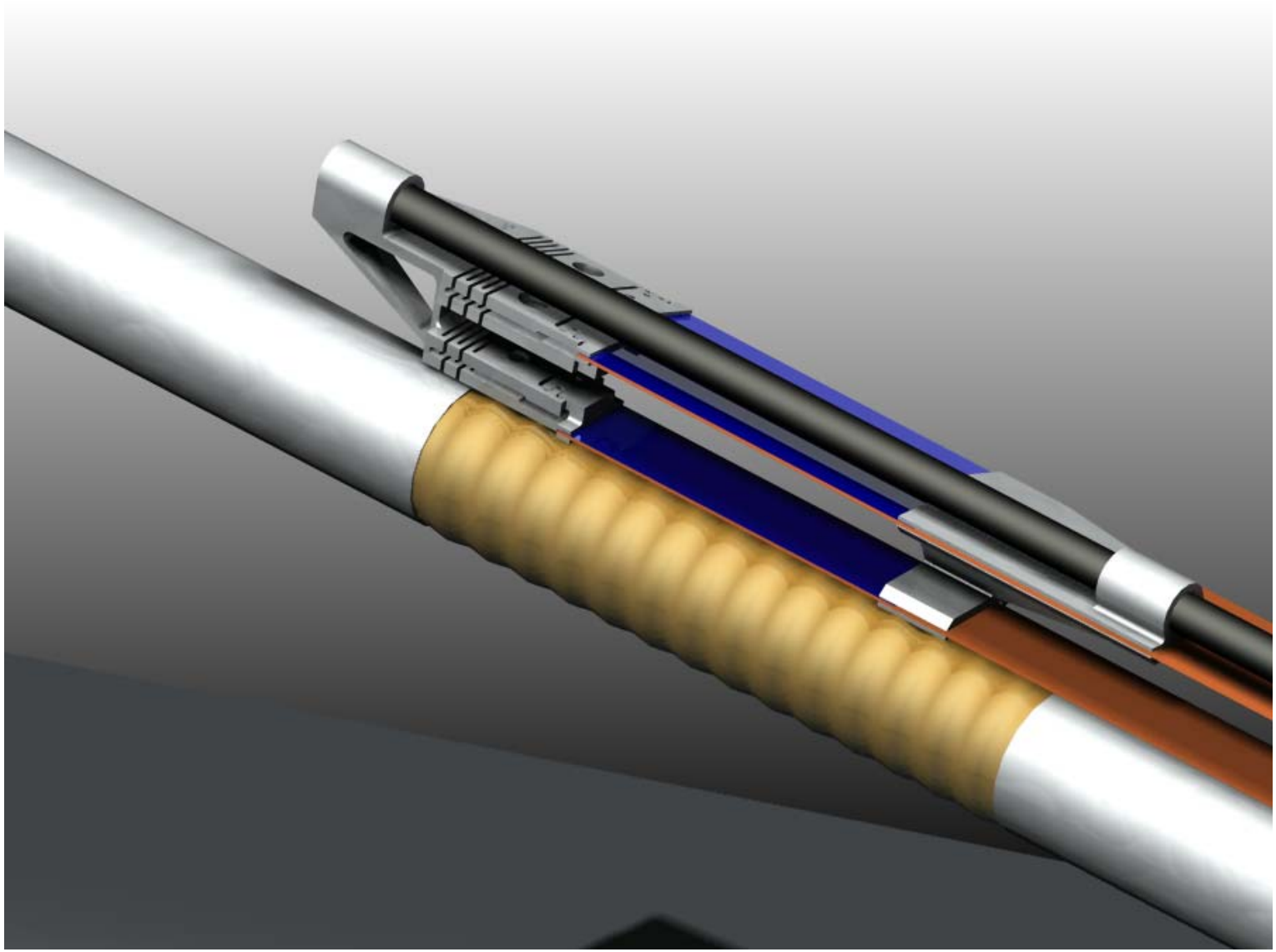
- Micro-vertex detector is being designed to go inside SVT
- It is being designed for rapid insertion and removal
- Should be flexible with a variety of detector designs

End of presentation

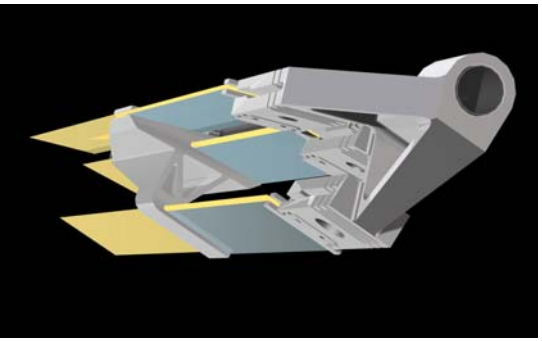
Tension concept

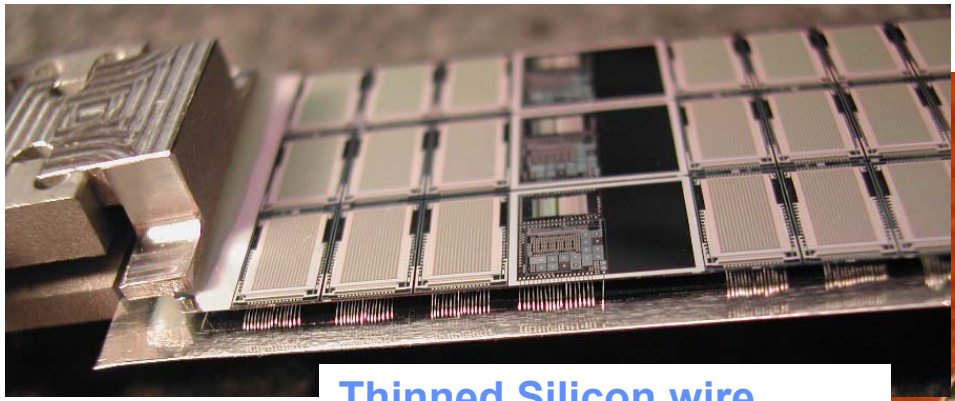


Tension concept

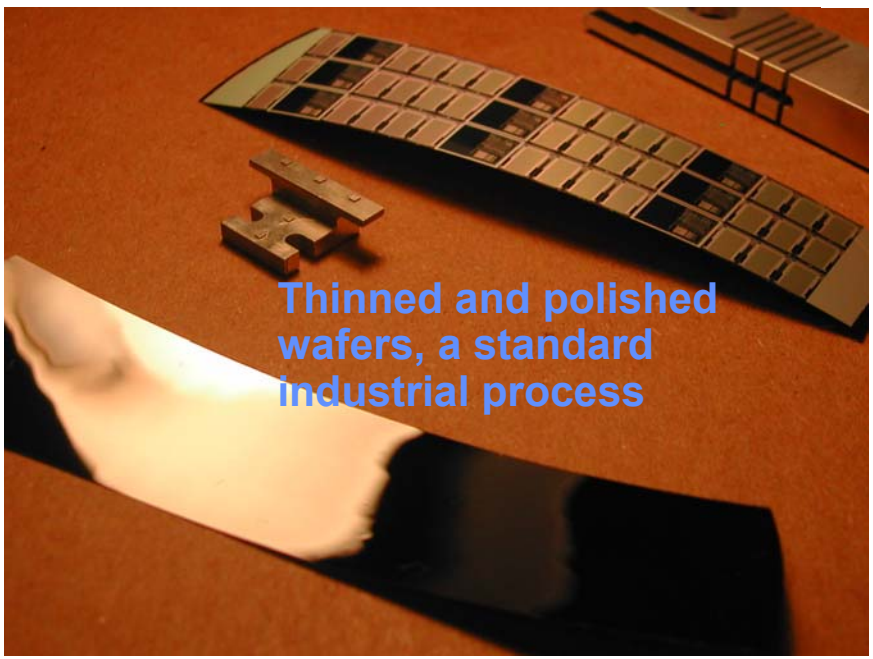


50 μm Silicon

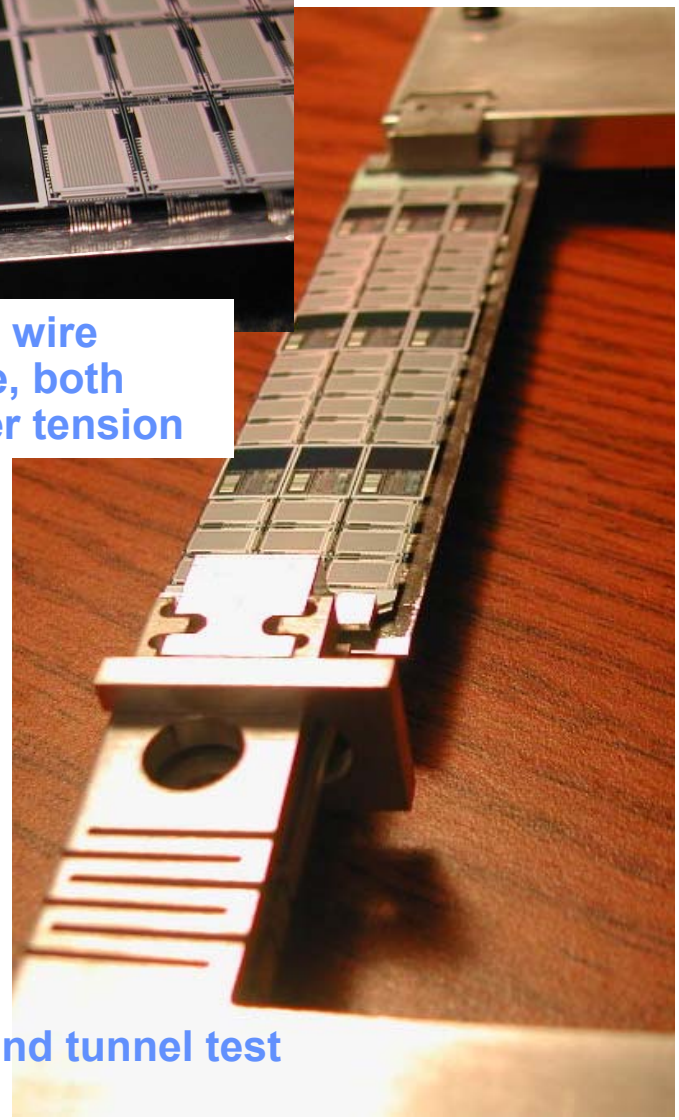




Thinned Silicon wire bonded to cable, both supported under tension



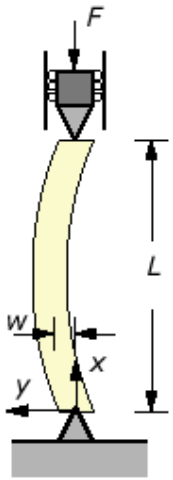
Thinned and polished wafers, a standard industrial process



Used in wind tunnel test

A thinner beam pipe

Elastic Bucking Instability
Euler 1757



Simply supported column subjected to axial load F

$$\frac{d^2}{dx^2}w + \frac{F}{EI}\cdot w = 0$$

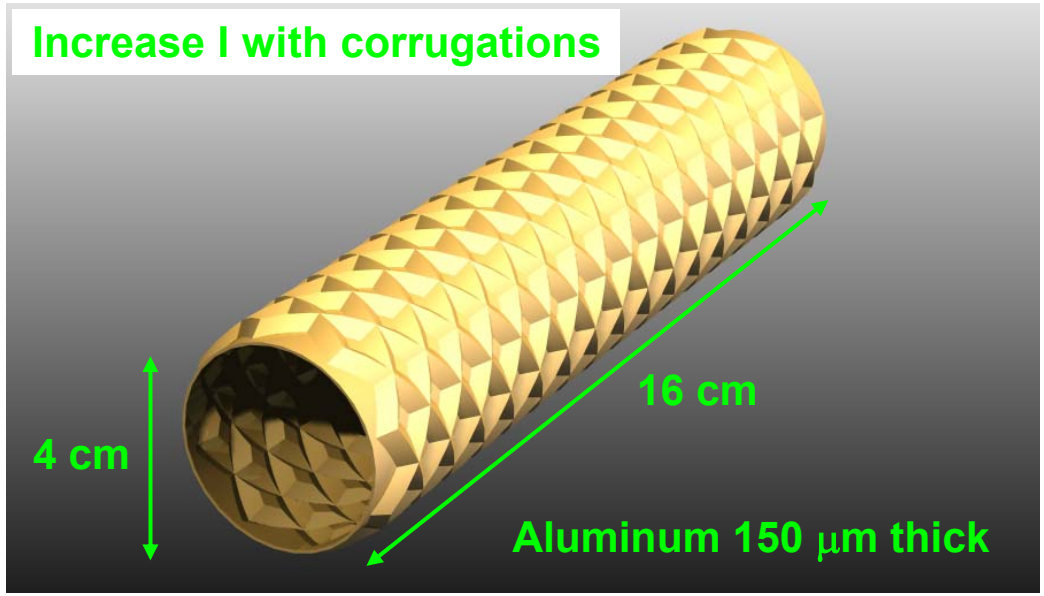
$$w(x) = A\cdot\sin\left(\frac{n\pi}{L}\cdot x\right)$$

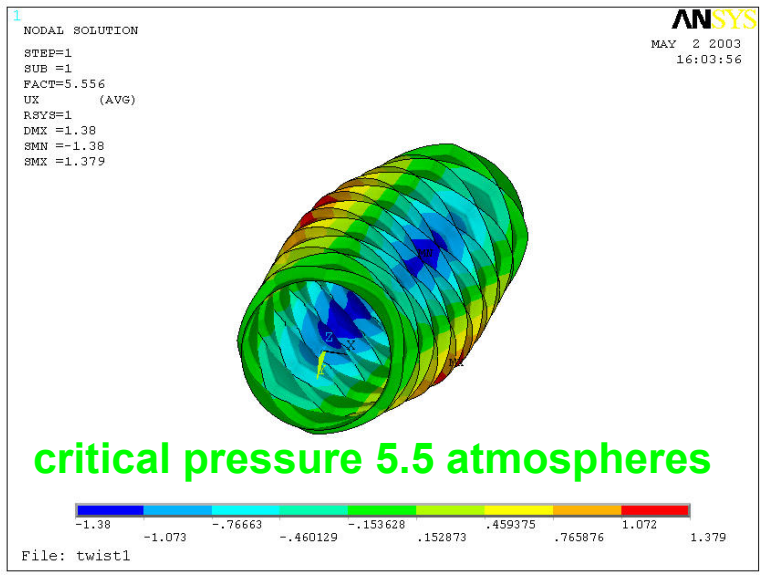
Eigen solution

$$F = EI\left(\frac{n\pi}{L}\right)^2$$

Critical buckling force

The challenge: increase moment of inertia along y without increasing material





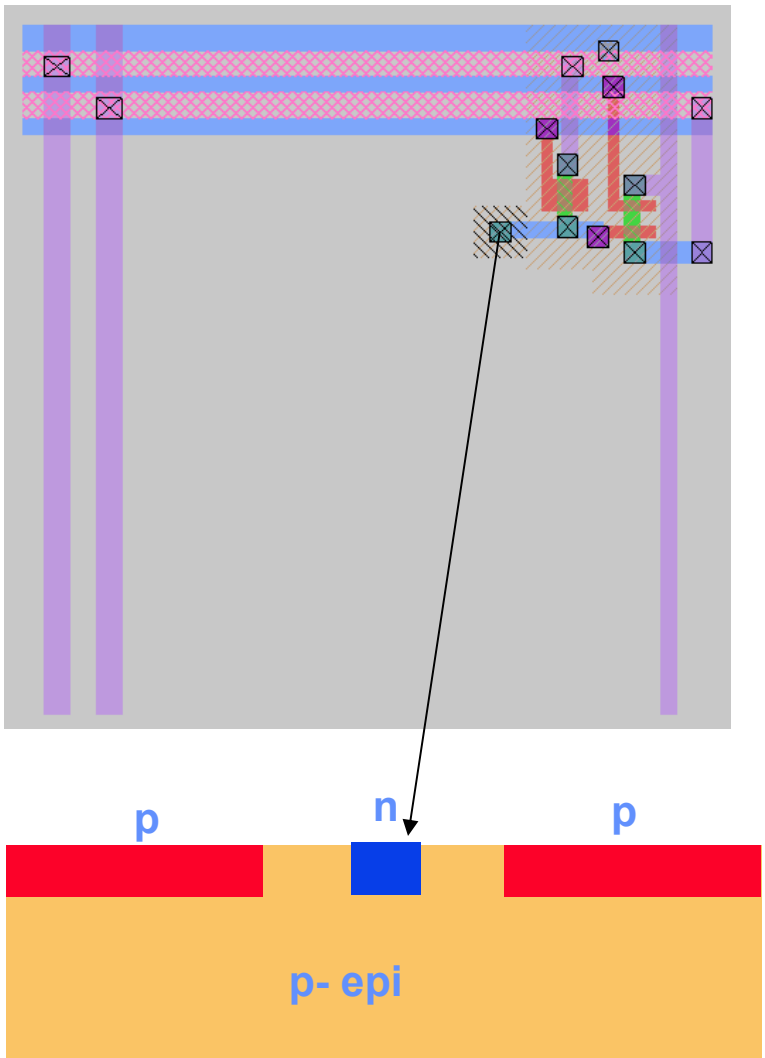
critical pressure 5.5 atmospheres

0.03 atmos. with no corrugation

Conclusion

- Present monolithic CMOS APS detector technology suitable for slow 10-20 ms readout (examples at LBNL/UCI and LEPSI/IRES)
- Fast readout not ready yet, but progress is being made
- Radiation hardness good enough for RHIC
- Mechanical concepts progressing
- R&D is fun, but…
- Proposal due this December

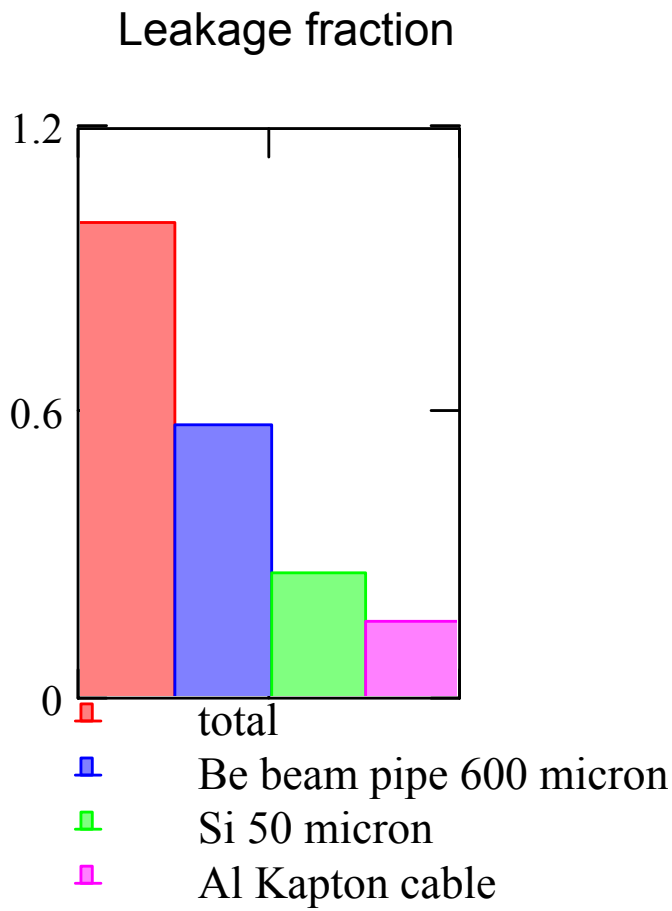
Test of diode variation



Puzzle:

- No Fe55 signal
- Will test with more statistics

Rejection of primary tracks

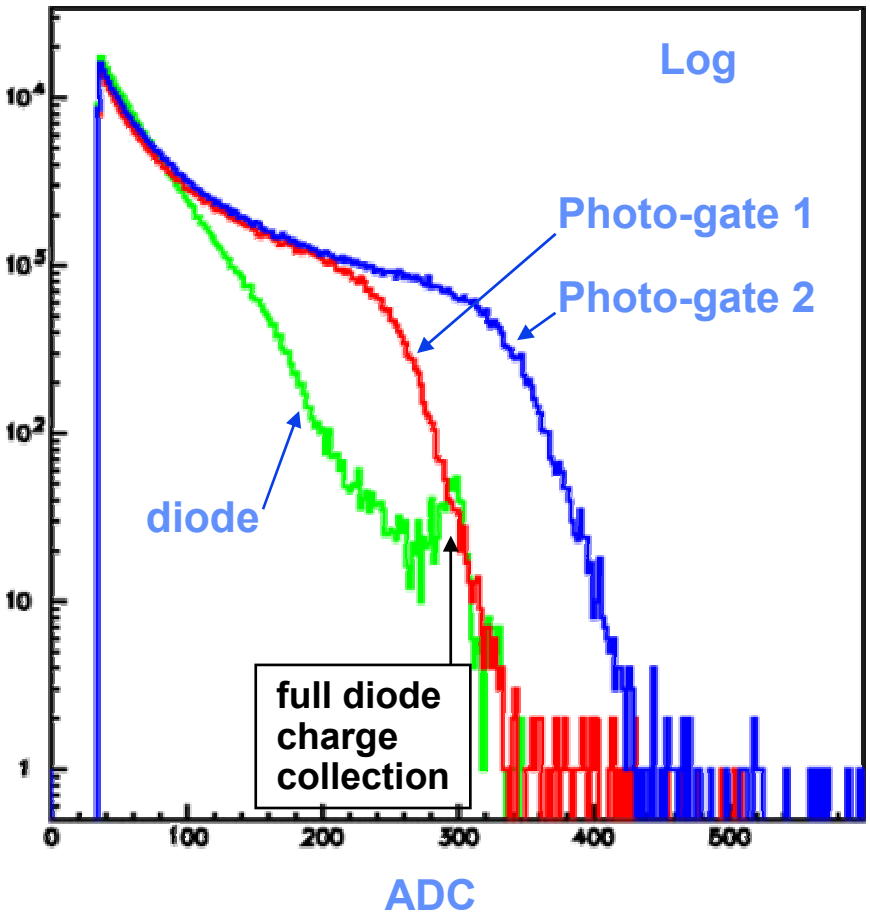


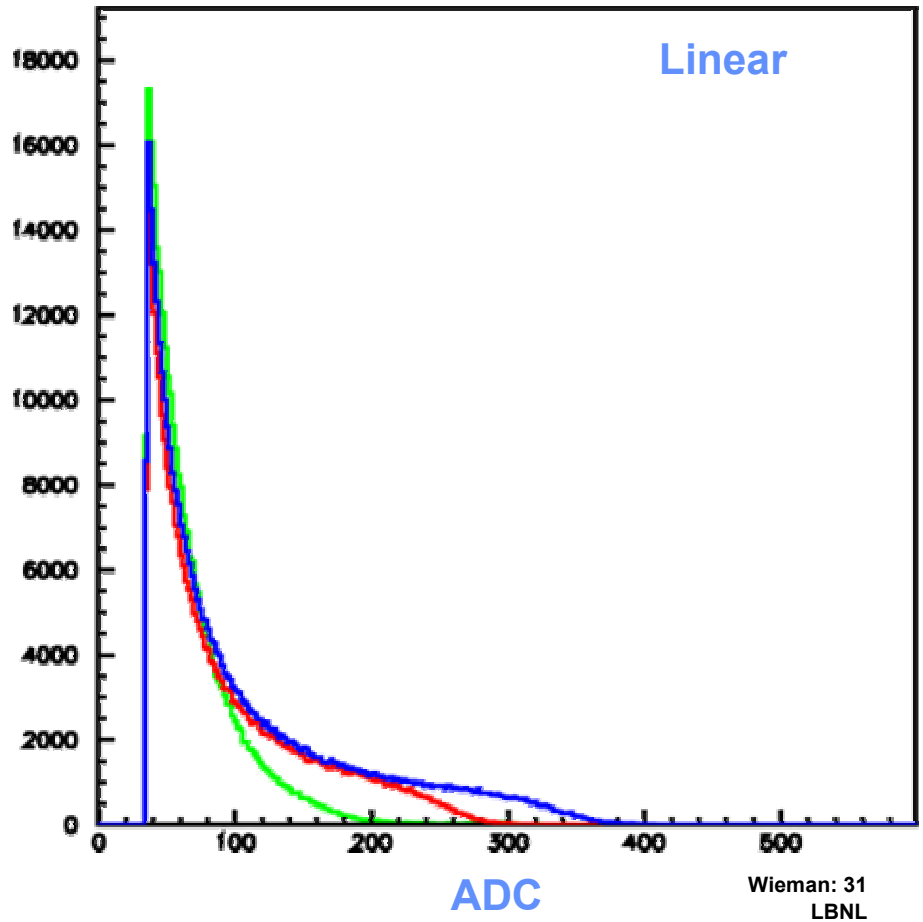
- **For large rejection ratios must set cut at several times multiple scattering angle**
- **At these large angles single coulomb scattering dominates and materials contribute linearly**

Beam pipe x/X0 = .17 %
Si x/X0 = .05 %
C Comp x/X0 = .03 %
Al Kapton x/X0 = .03 %

Photo-gate Fe^{55} X-Ray test

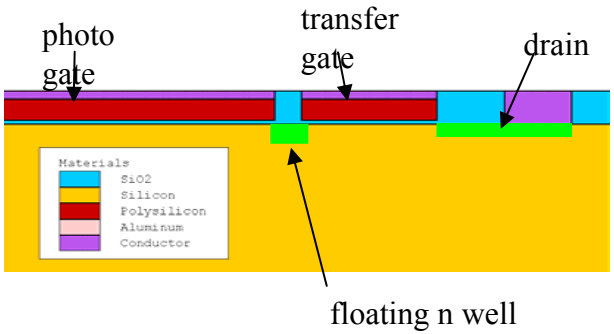
- Charge collection histogram for CMOS APS – comparing two photo-gate structures to standard diode structure
- Photo-gate coupled directly to drain – no transfer gate
- Photo-gate shows more complete charge collection, but…



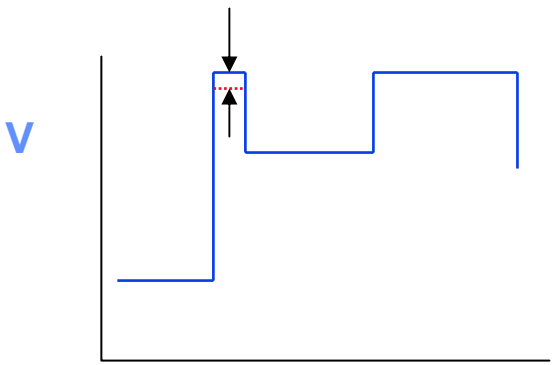


Drain current after light injection, floating n well delay

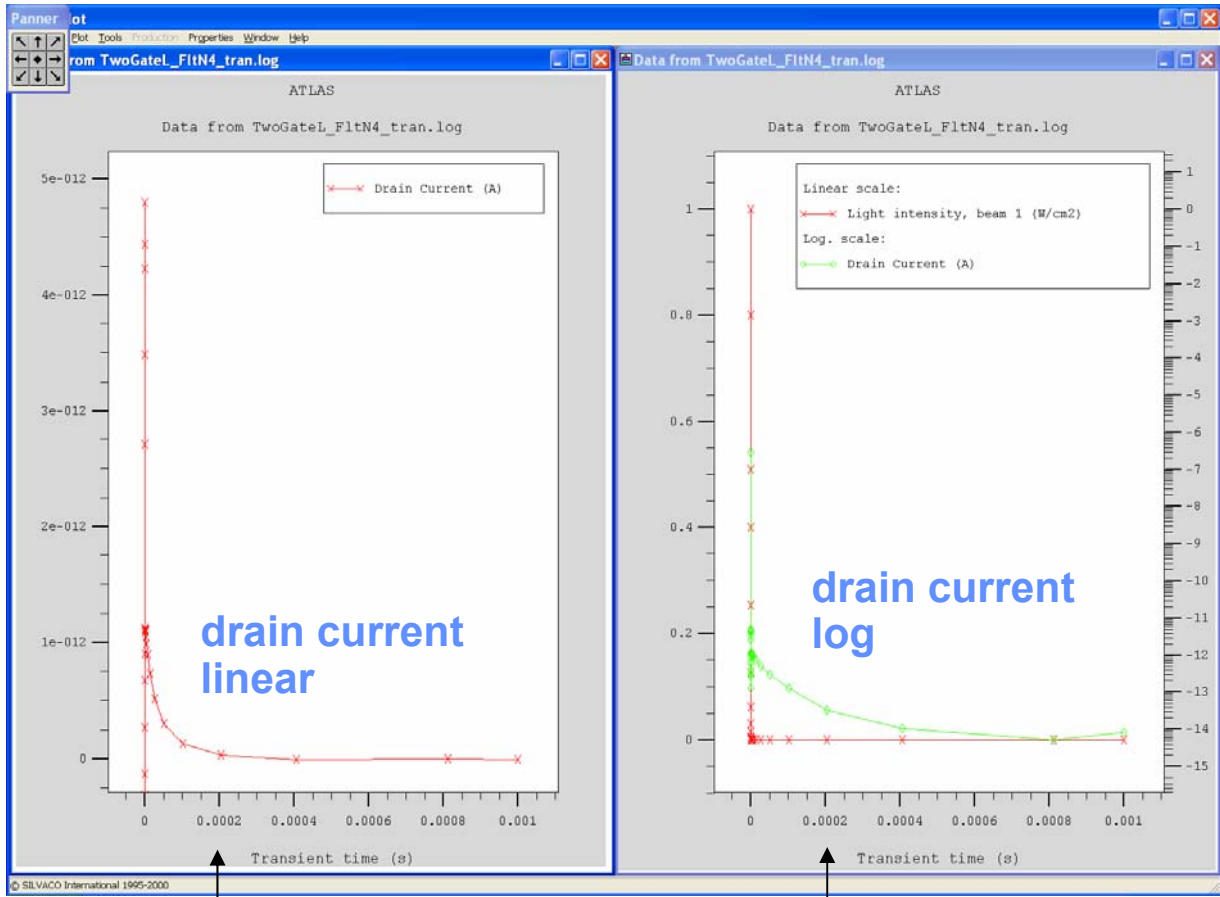
Light injection



$\Delta V = Q/C$ **(very small)**



Potential before and after injection



Smaller the signal the higher the effective resistance and the slower the transfer

200 μs

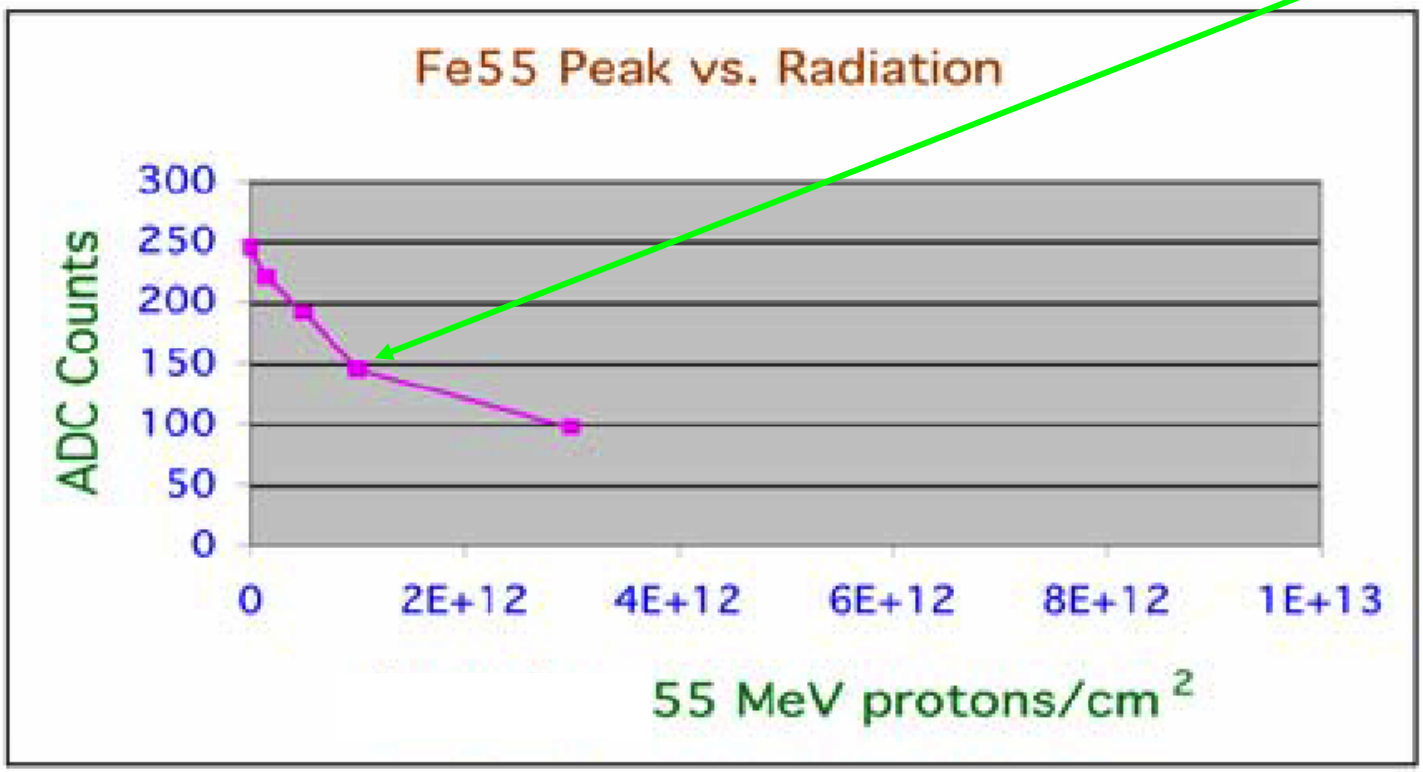
200 μs

Radiation resistance

- **Radiation tests of the LBNL APS at the 88” cyclotron**

  55 MeV protons

30 year RHIC operation at 4 x design luminosity



Properties, LBNL APS

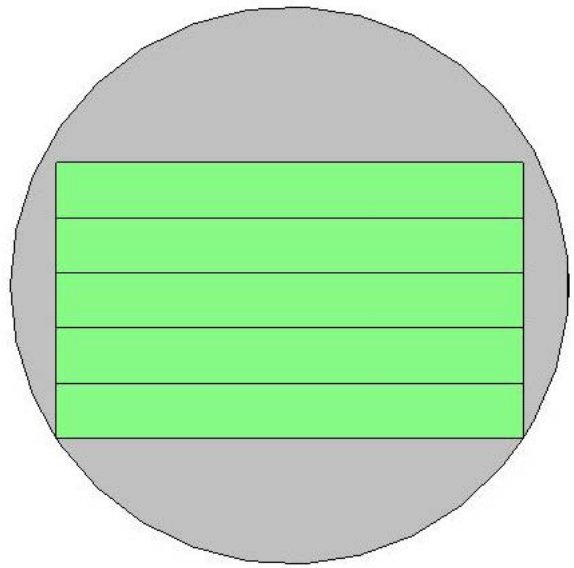
MIP (most probable)	440 e
Node C, measured with Fe^{55} Xray	6.1 fF
Gain	~26 μV/e
Noise (1 pixel, CDS, I_{leak} subtr)	17 e rms
Signal/Noise (9 pixel sum, CDS)	9
Signal/Noise (potential, single pix)	26
kTC reset noise (measured)	50 e rms
kTC reset noise (expected)	30 e rms
Leakage Current	0.9 fA

Silicon Cost

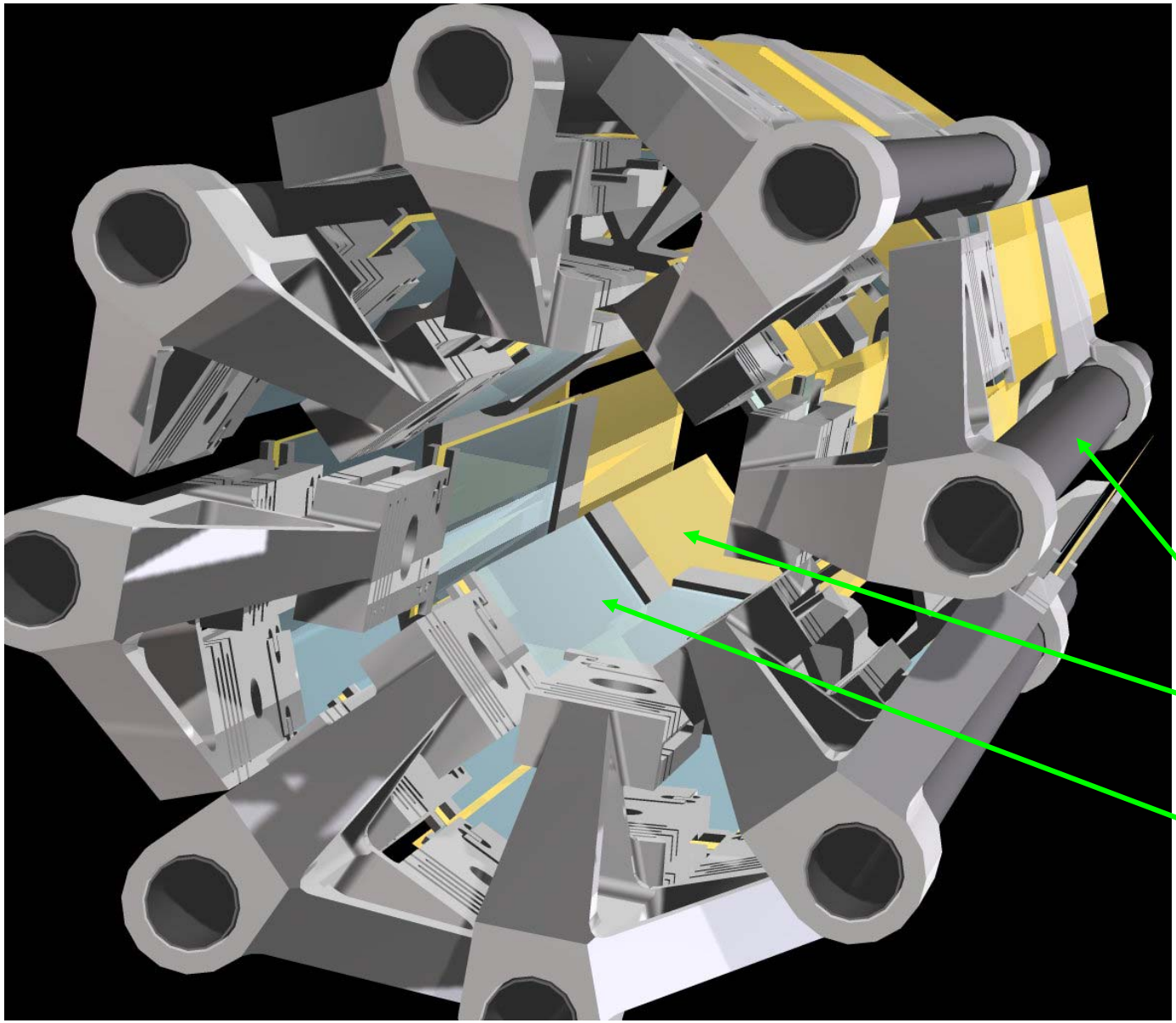
Ladders per Wafer	5
Ladders per Detector	24
Yield	60%
Number of Detector Copies	4
Number of Wafers	32
Wafer Cost Each	2-5 k$
Wafer Costs	64-160 k$
Mask Cost	150-200 k$
Total	214-360 k$

8 inch wafers

20 mm x 170 mm ladders



Mechanical Concept



- **Single end support for rapid installation and removal**
  - For beampipe bake out
  - Insurance for beam excursion damage
- **Readout electronics in end support module**